EUV Mask Readiness for High Volume Manufacturing

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Intel Corporation

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Outline

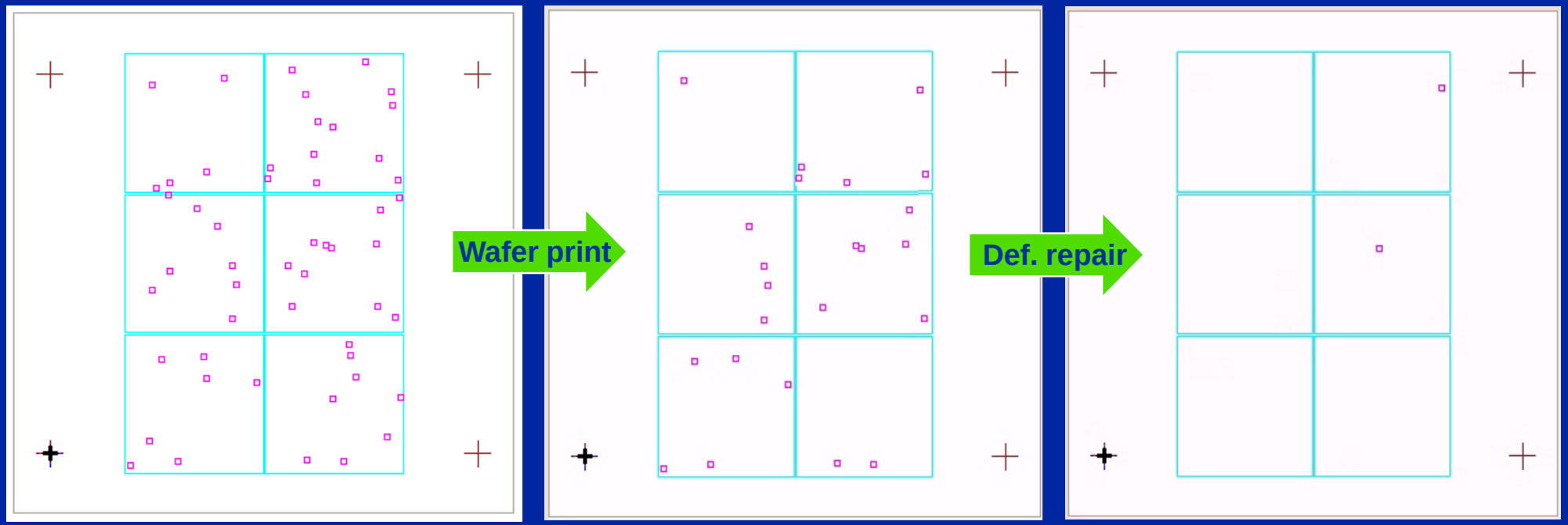
- Defect reduction
- Mask patterning
- Absorber options
- Mask handling
- Summary

Zero Defect Challenge: 32 nm SRAM Test Chip

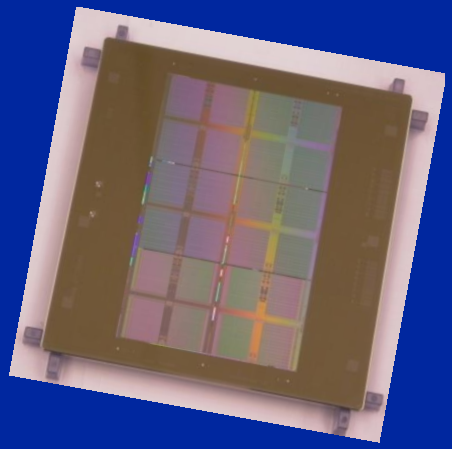
50 defects on mask insp.
(90nm pixel)

23 printable defects
(10+% ΔCD)

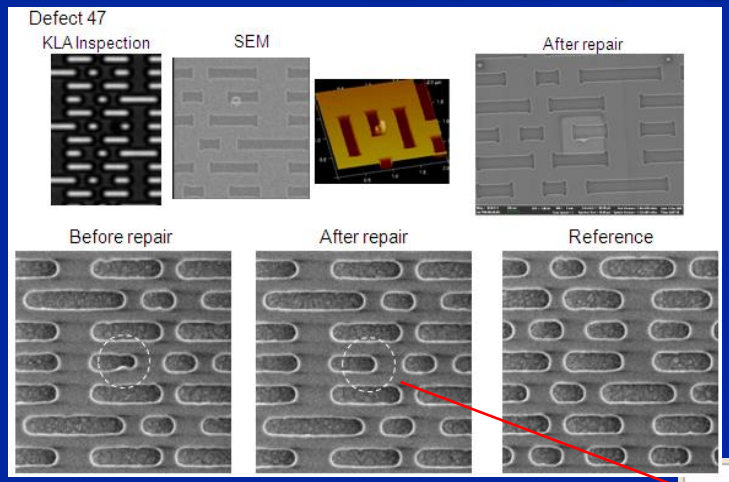
21 defects fully repaired

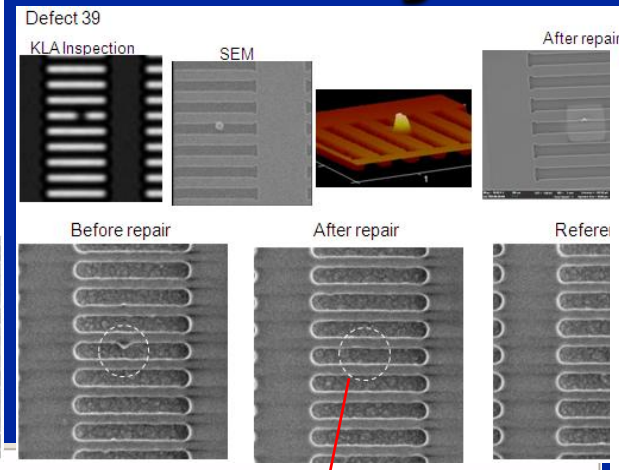


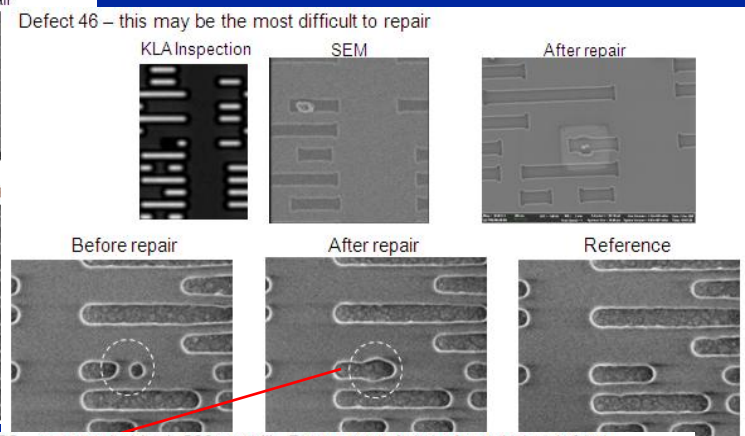
- **Ru capped ML blank**
- **Intel TaON/TaN absorber**
- **Resist A process**
- **70 nm inspection sensitivity**
- **14 of 23 printable defects traced back to blank defects**

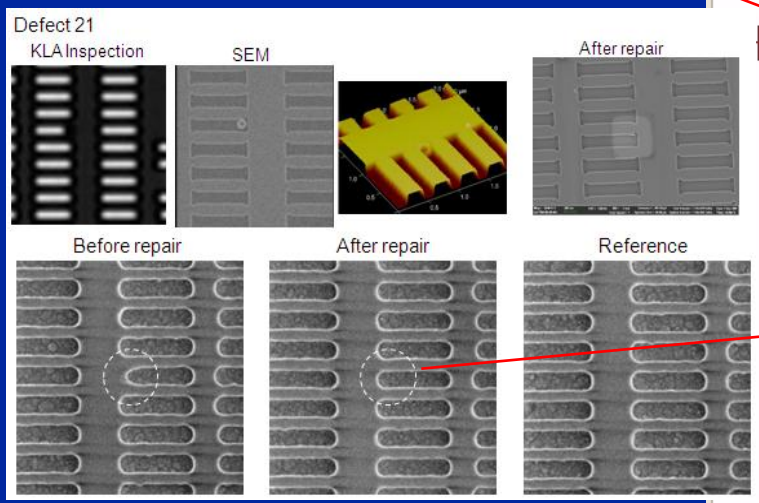


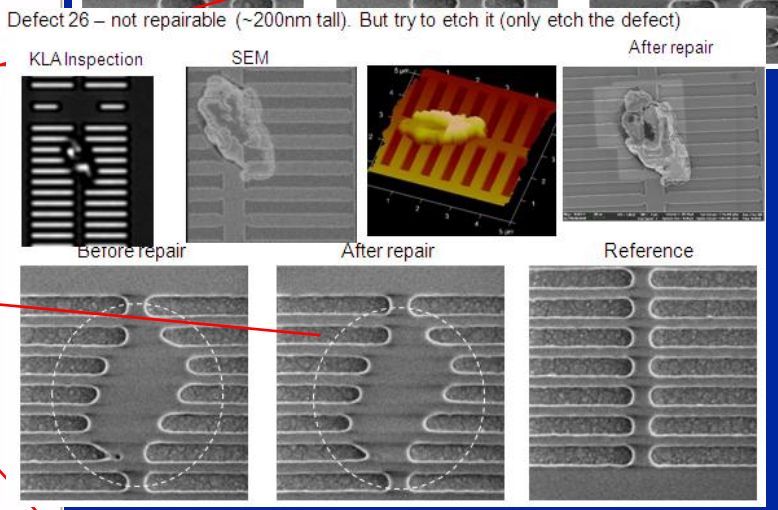
21 Defects Fully Repaired

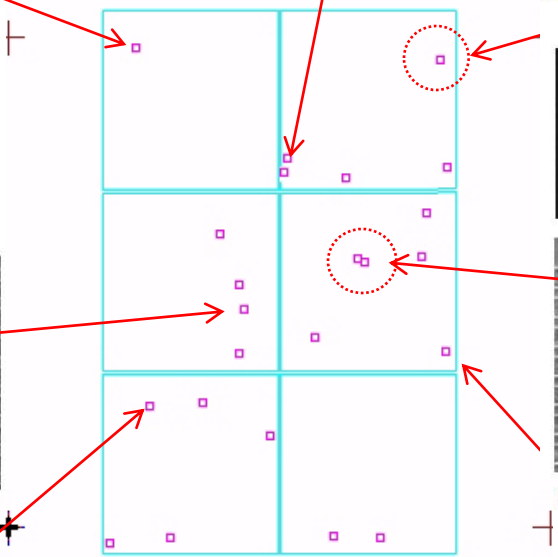


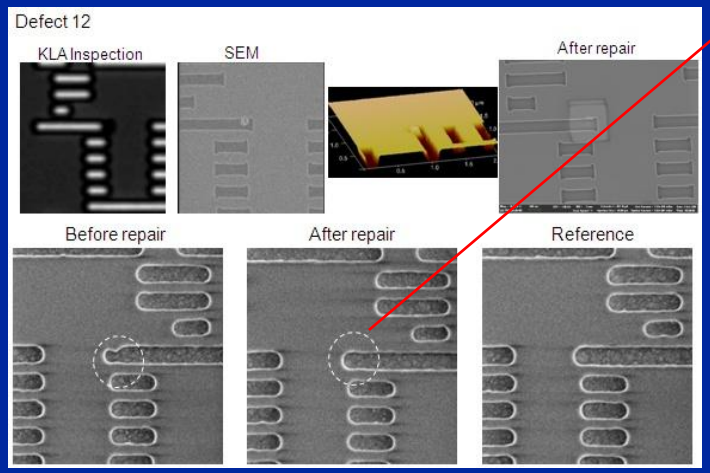


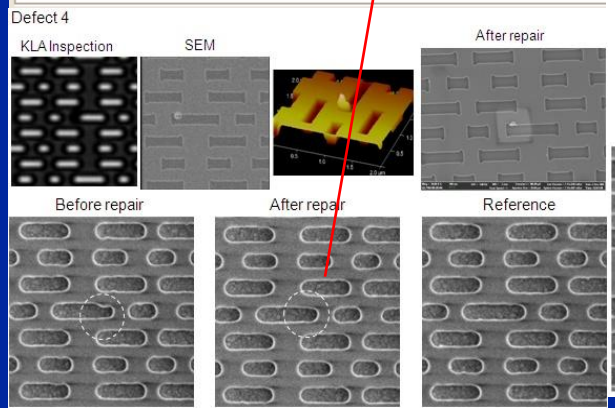


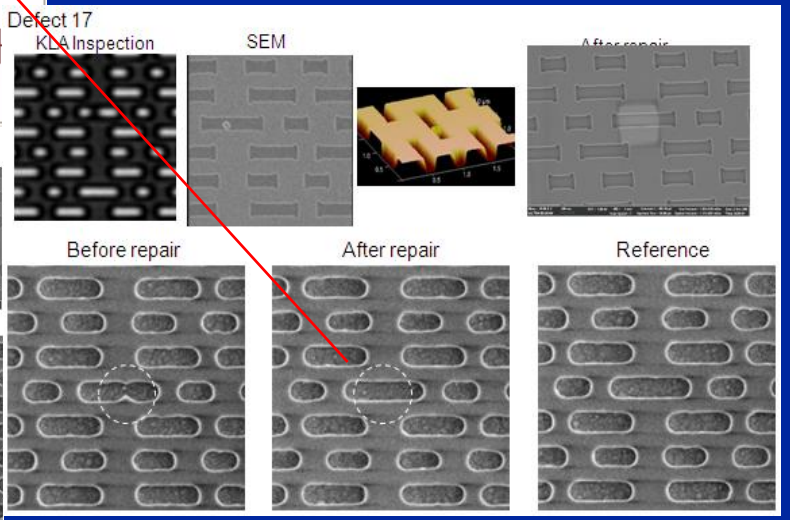






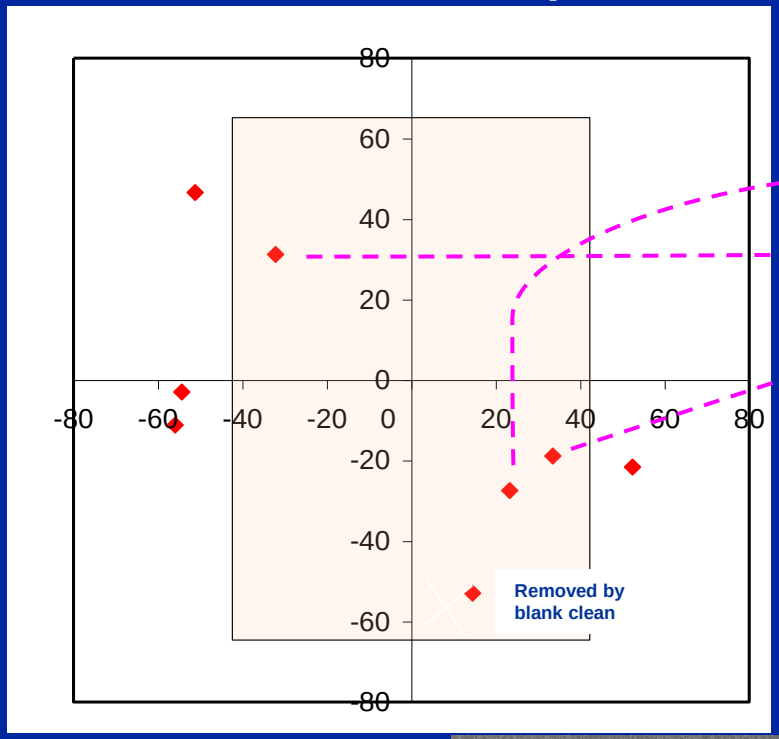




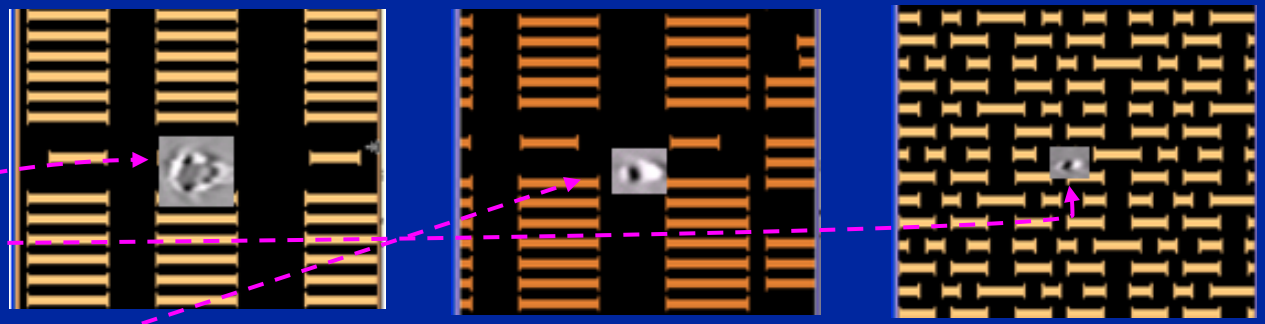


ML Defect Mitigation: Three Defects Hidden by A Single Pattern Shift

Blank defect map

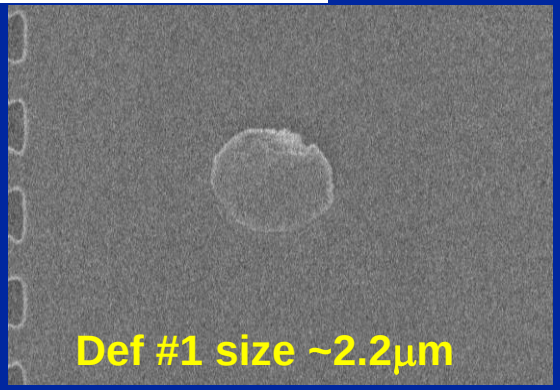


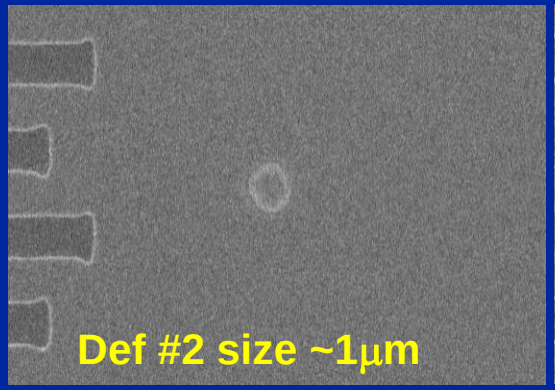
No pattern shifting: Defects land at active areas

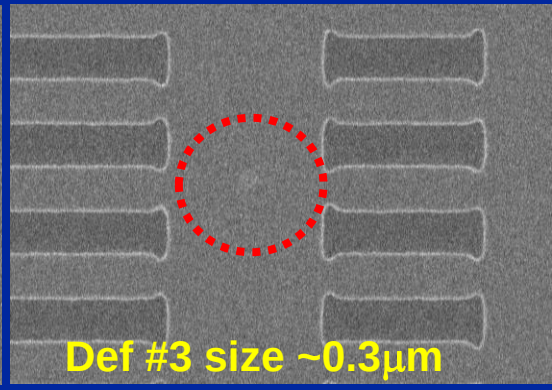


With shifting: Defects are buried in inactive areas

- 32 nm SRAM
- Intel TaON/TaN absorber

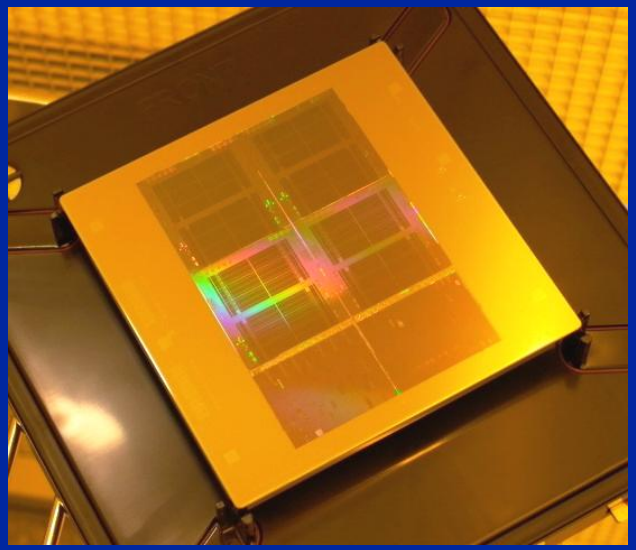


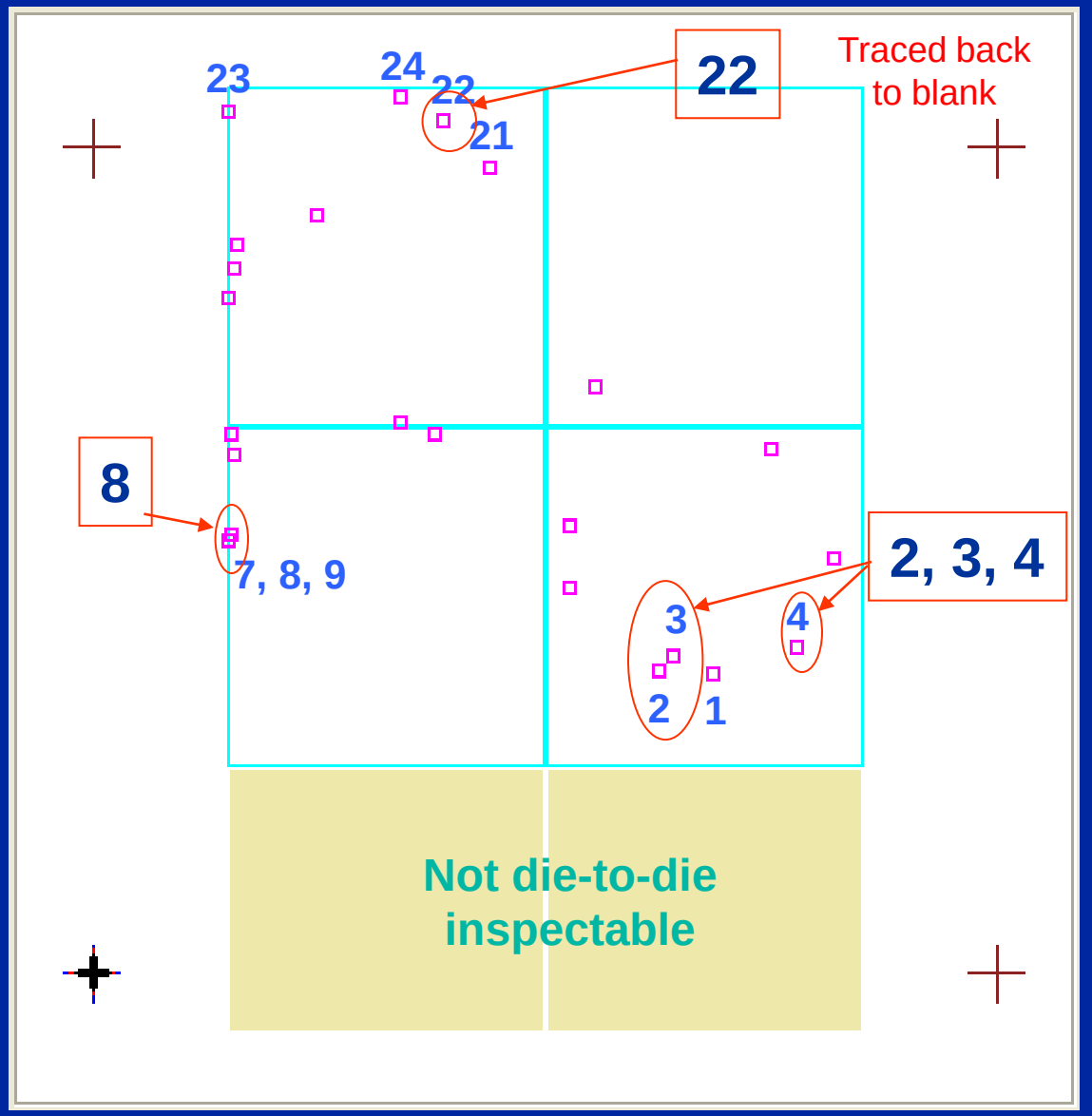




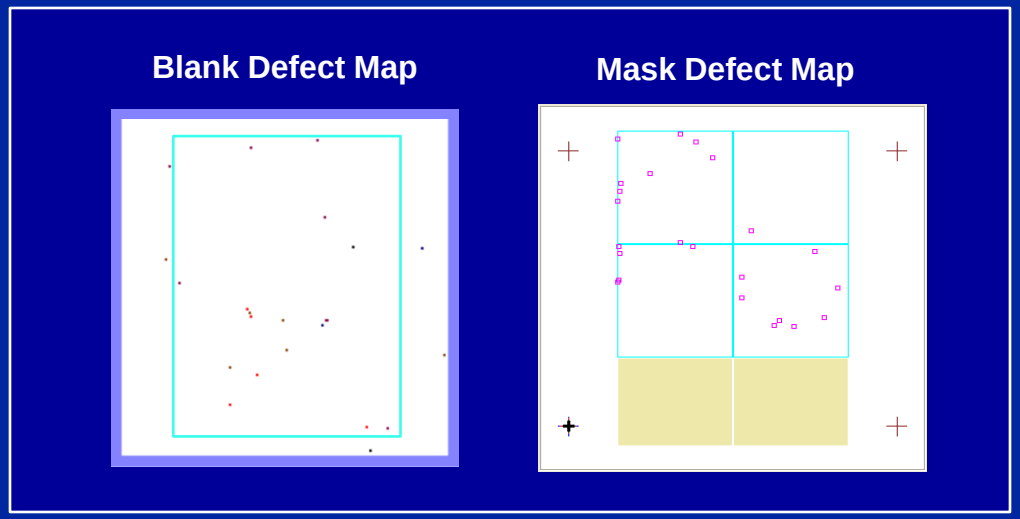
Zero Defect Challenge: 22 nm SRAM Test Chip

- Ru capped ML blank
- Supplier's absorber
- Resist B process
- 50 nm insp. sensitivity
- 5 of 24 mask defects traced back to blank





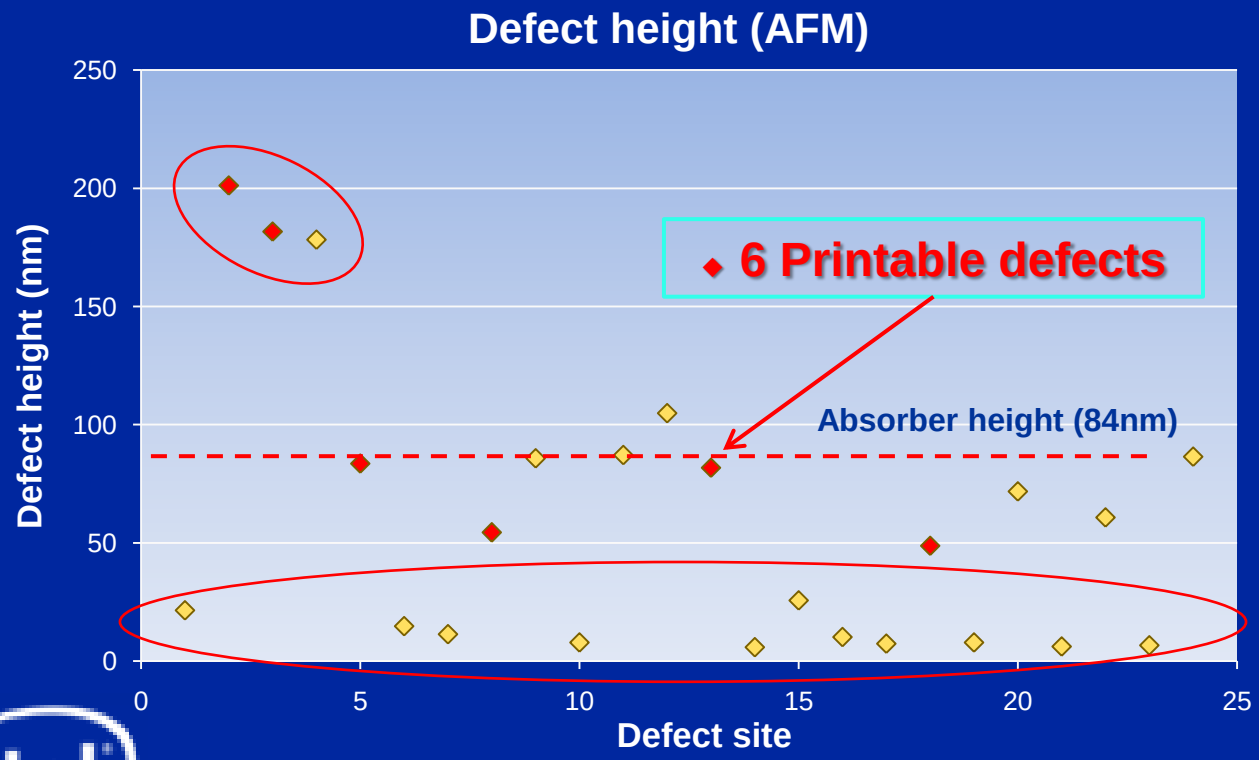
Defect Characterization



5 traceable to abs. blank

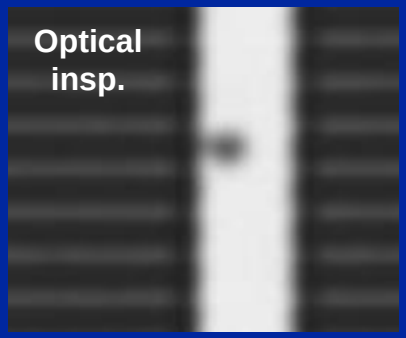
8 selected for repair

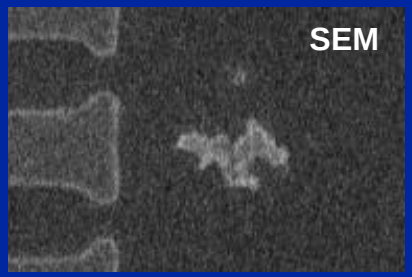
Defect ID	AFM Defect Height (nm)	Printable Defect
1	21.5	N
2	201.2	Y
3	181.7	Y
4	178.3	N
5	83.6	Y
6	14.8	N
7	11.4	N
8	54.4	Y
9	85.8	N
10	7.9	N
11	87.2	N
12	104.9	N
13	81.8	Y
14	5.9	N
15	25.7	N
16	10.2	N
17	7.4	N
18	48.8	Y
19	7.9	N
20	71.8	N
21	6.2	N
22	60.8	Y
23	6.7	N
24	86.5	N

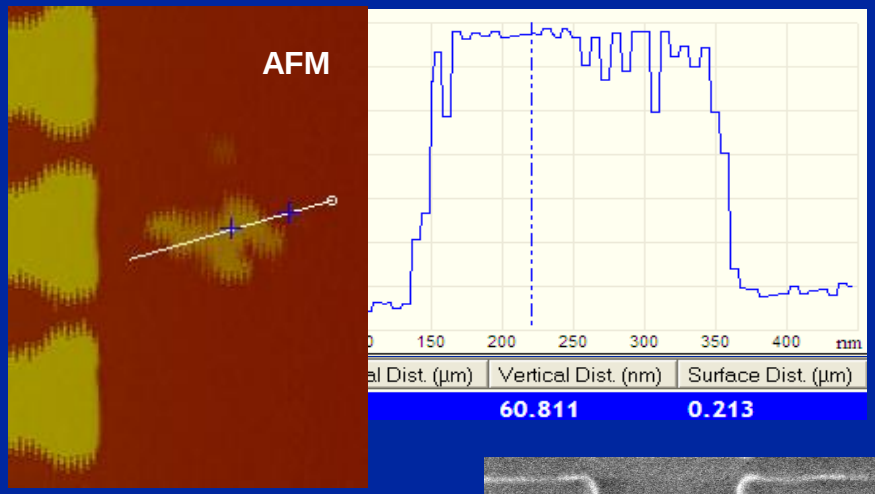


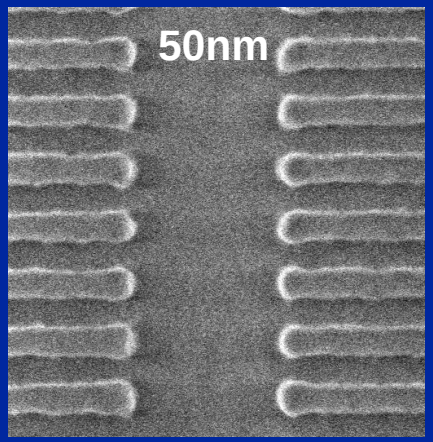
Non-Printable Defect s Can Become Printable

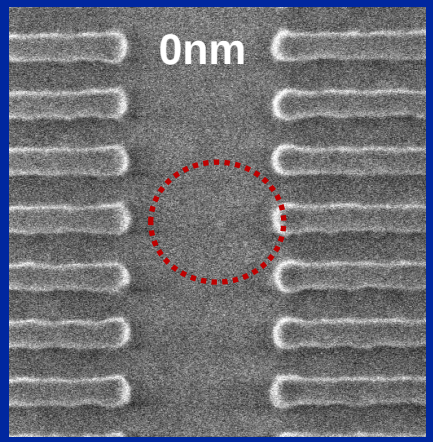
Mask Insp. & char.

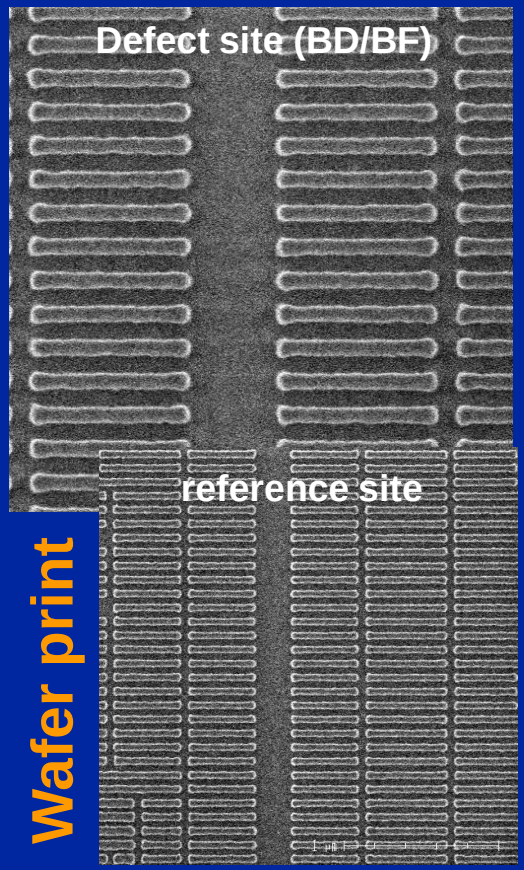






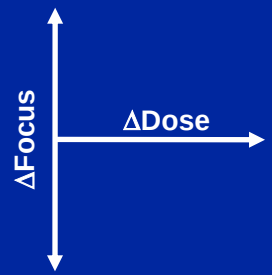


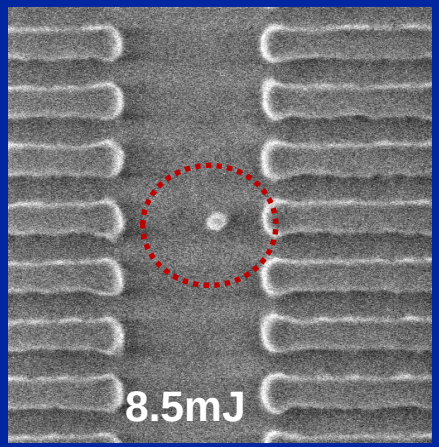


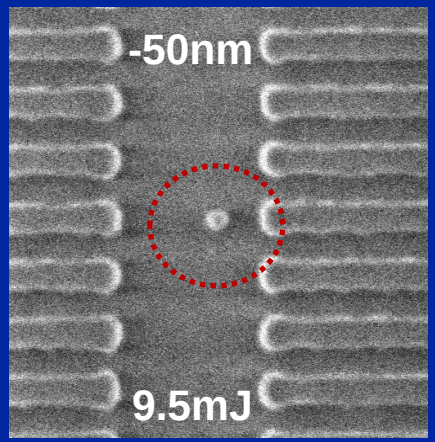


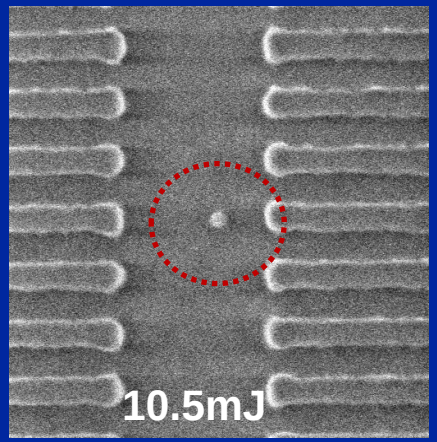
Wafer print

D/F matrix in wafer Print

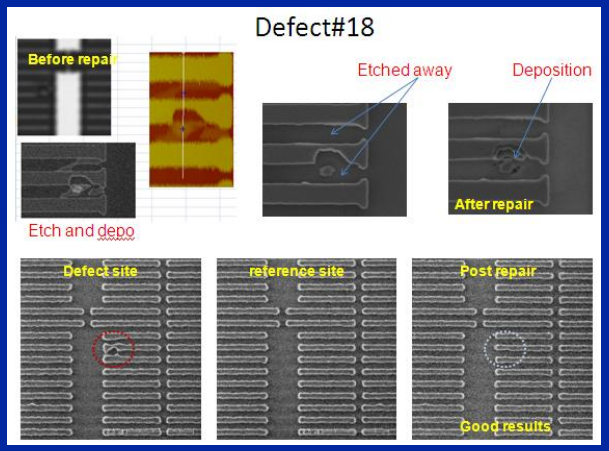


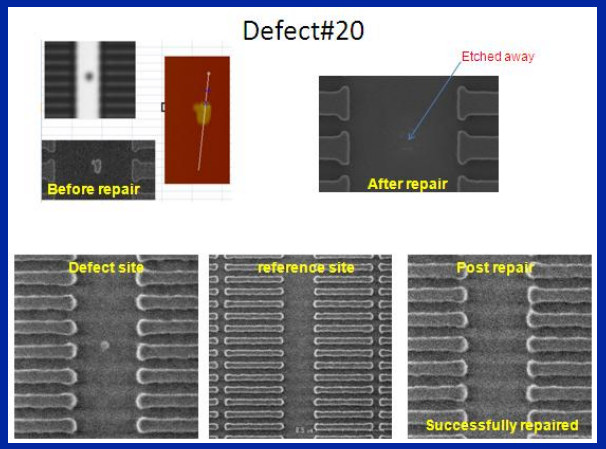


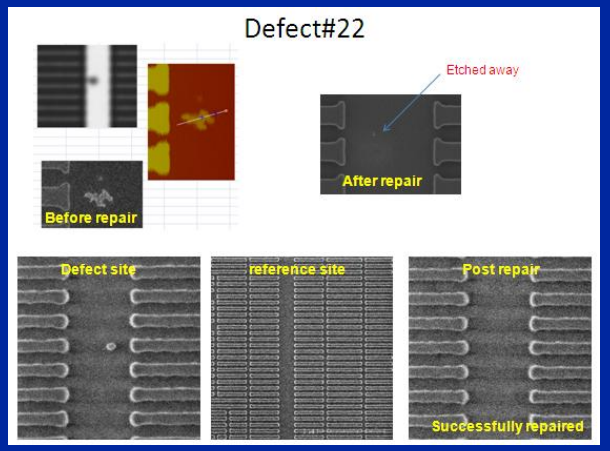


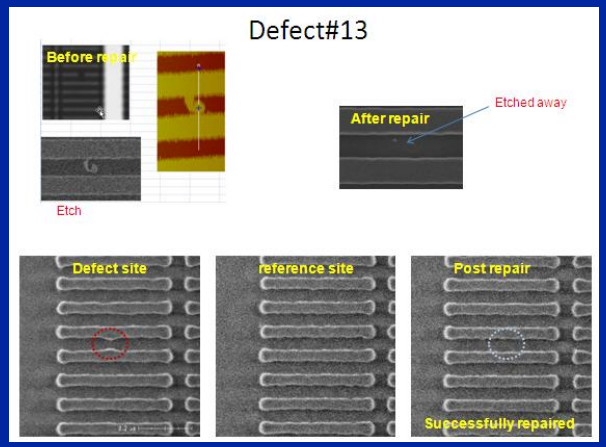


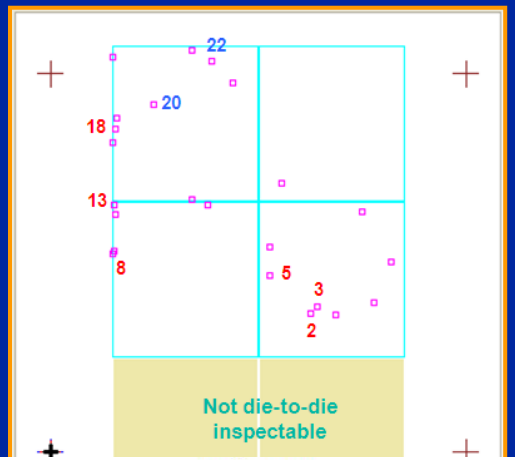
Successful Repairs

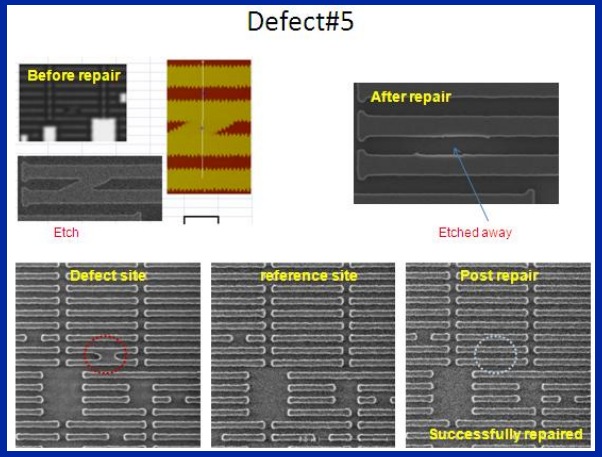


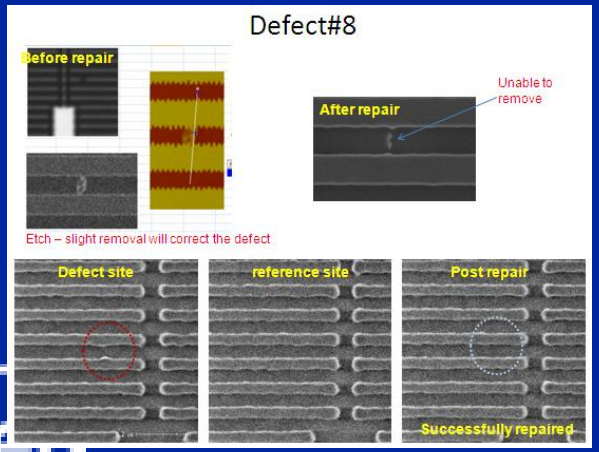


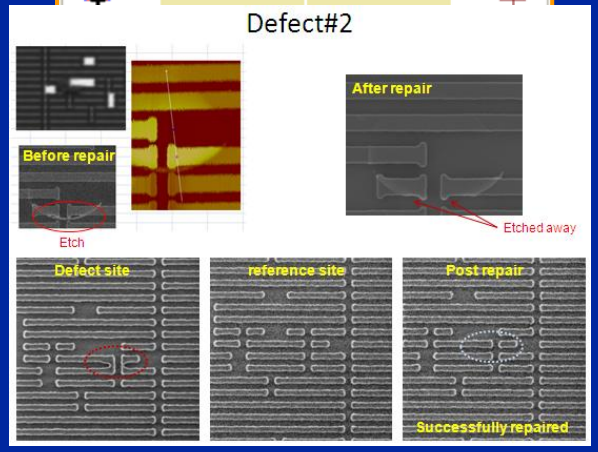


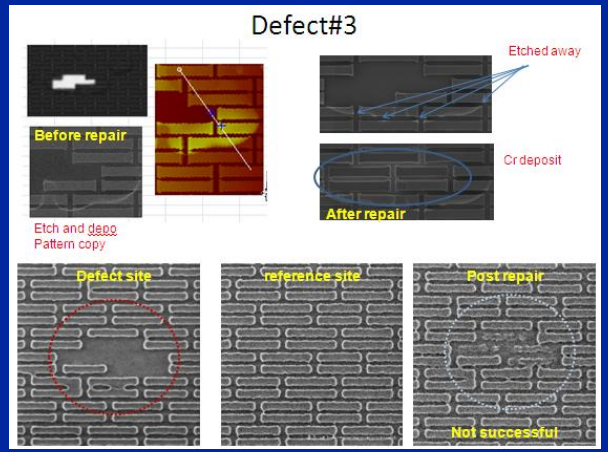








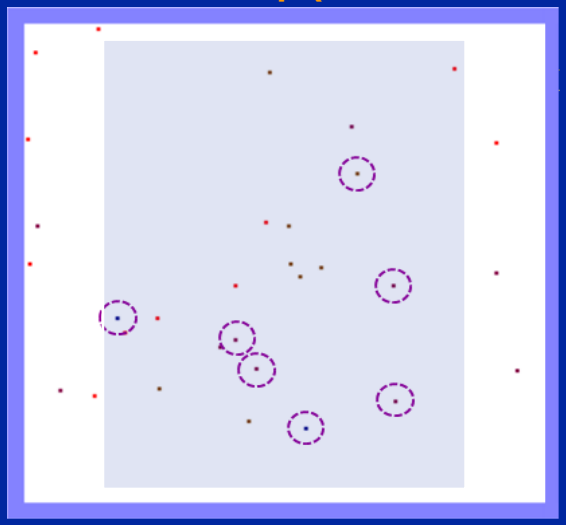


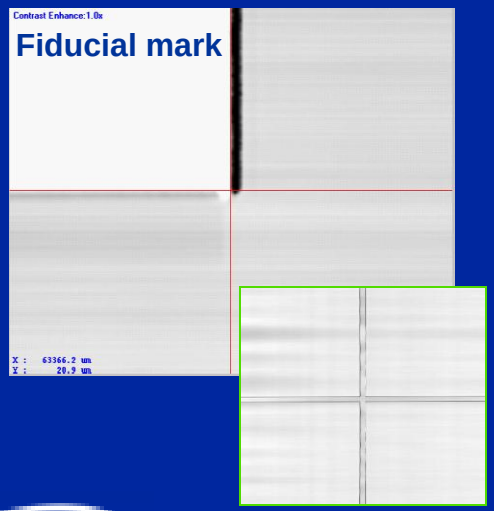


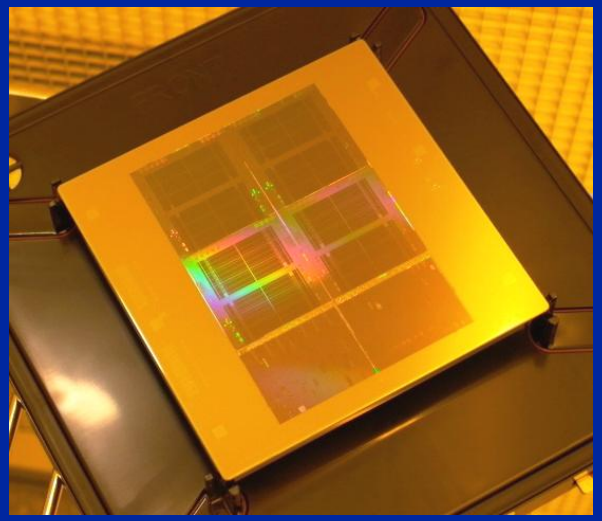
Mitigation for Multiple ML Defects on 22 nm Device Layer

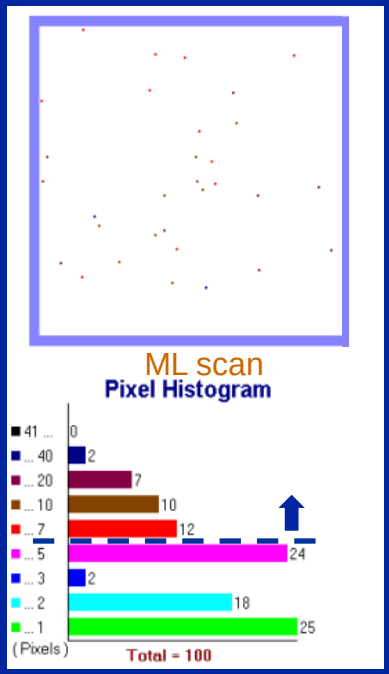
- Supplier ’s absorber
- Fiducial marker in absorber
- Precise coordinate measurement
- 7 ML defects selected based on traceability
- E-beam writer 2nd layer overlay capability

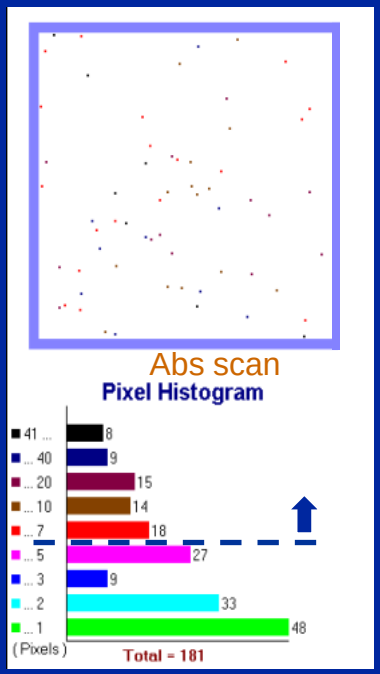
Blank defect map (ML/Abs –AND)



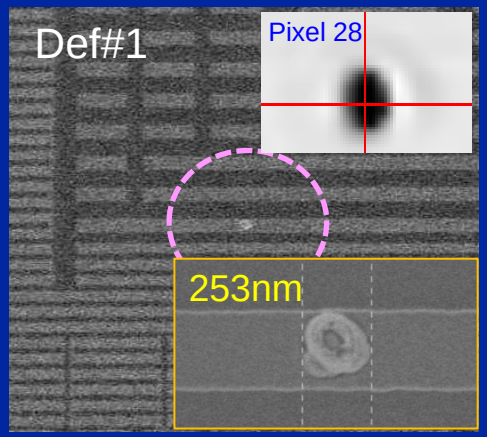


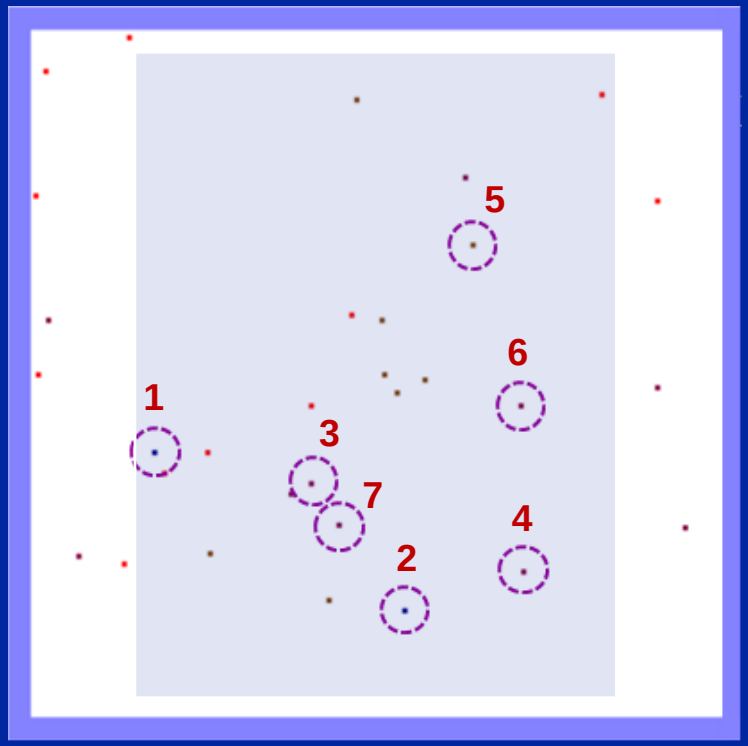


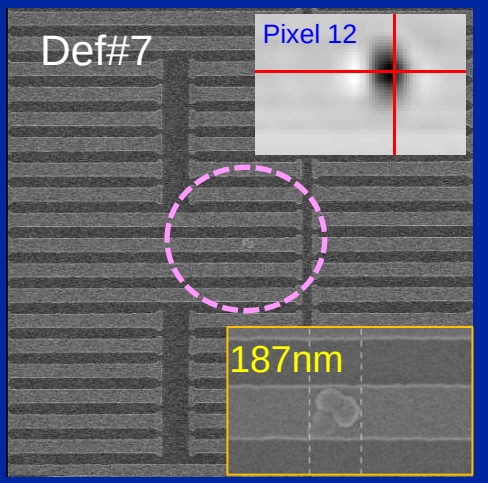


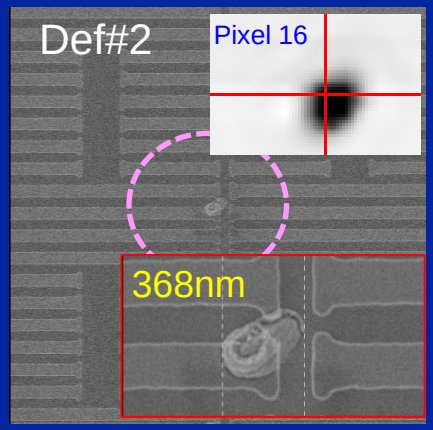


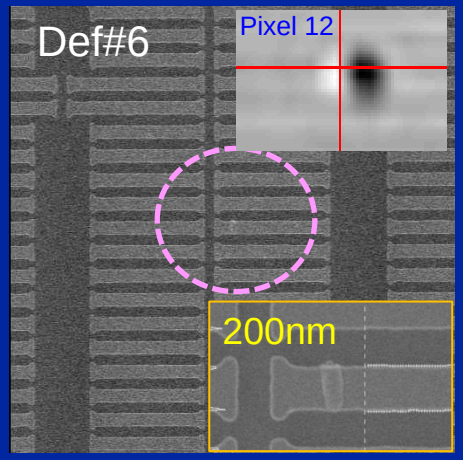
Mitigation Results on Mask

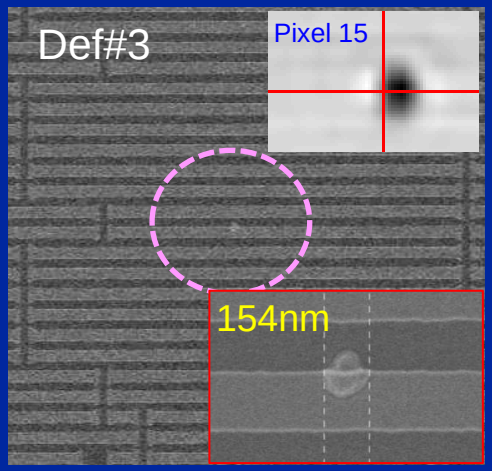


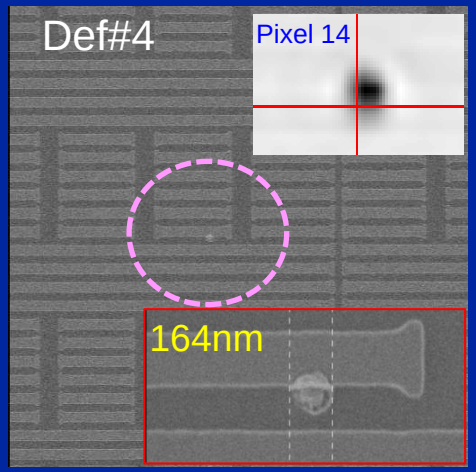


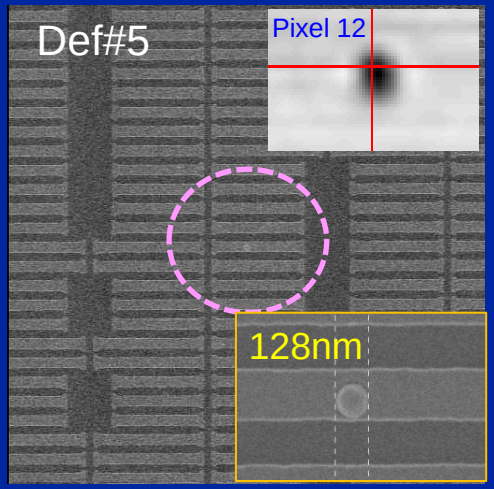




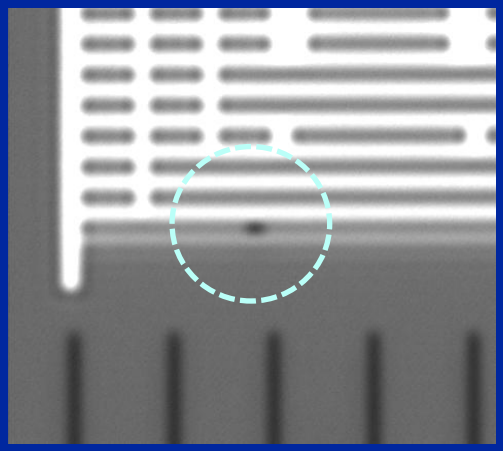




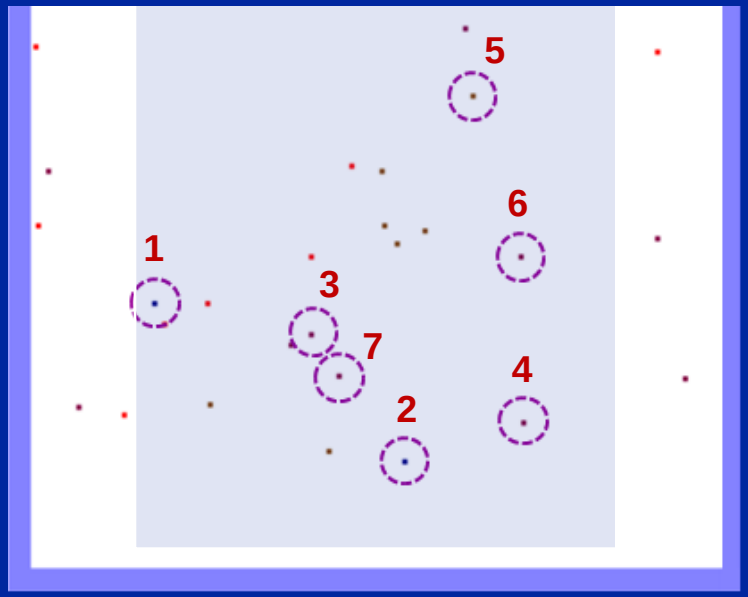


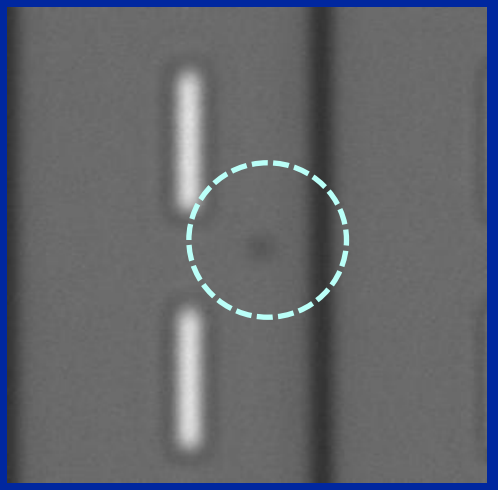


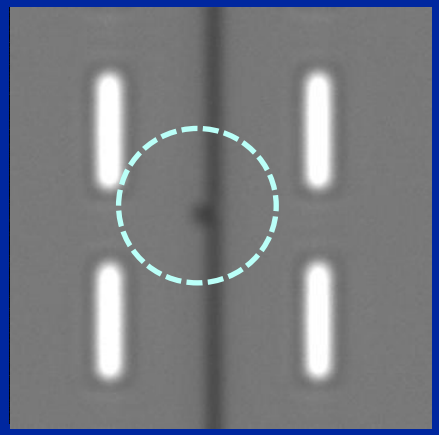
Mitigation Results on Mask

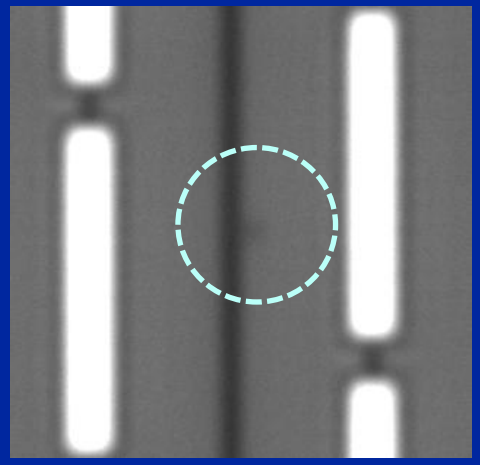


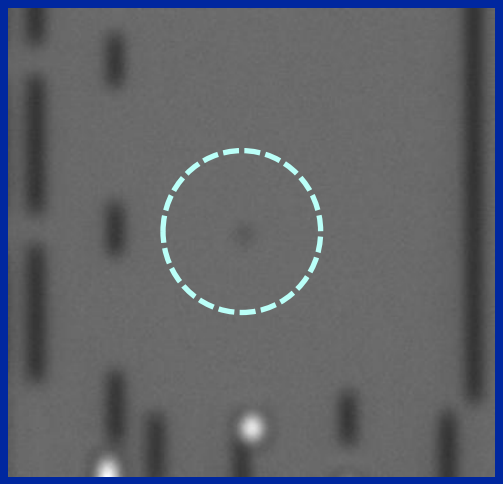
- 4 ML defects fully hidden
- 3 ML defects partially covered
- w/o pattern shifting: only 1 ML defect can be naturally buried

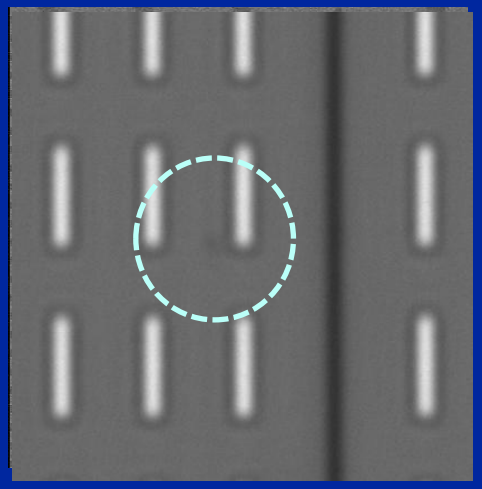


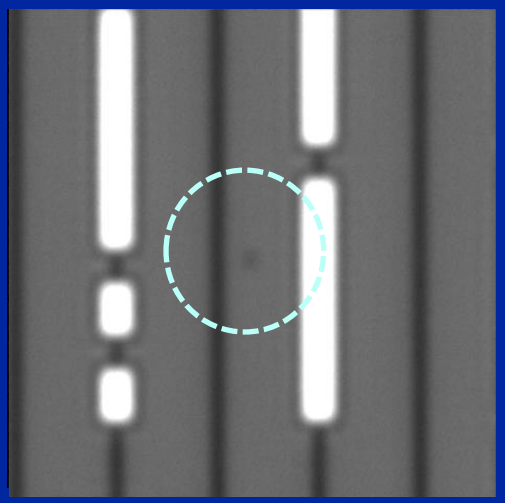












WI Defect Source Analysis

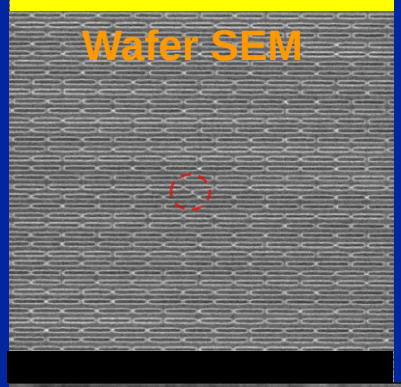
WI repeater number	Detected by LTEM **substrate** inspection (M1350 λ=488nm)	Detected by as received **ML** inspection (M1350 λ=488nm)	Detected by post **absorber** deposition inspection (M1350 λ=488nm)	Detected by **reticle** inspection (λ=257nm)	Detected by Adv. **reticle** inspection (λ=193nm)	Detected by LBNL **AIT** (λ=13.5nm)
1	yes	yes	yes	no	no	
2	no	yes	yes	no	no	
3	no	no	no	yes	yes	
4	no	no	no	yes	yes	
5	yes	yes	yes	yes	yes	
6	no	no	no	no	no	yes
7	no	no	no	yes	yes	
8	no	yes	yes	no	no	
9	no	no	no	no	no	yes
10	no	no	no	yes	yes	
11	no	yes	no	no	no	
12	yes	yes	yes	no	no	
(cluster)13	no	yes	yes	no	no	yes
14	yes	yes	yes	no	no	

- *32 nm device layer mask*
- *5 of 14 repeaters detected in the mask inspection.*
- *11 of 13 repeaters & "defect cluster" were detected by one or more means*
- *2 repeaters where not assignable to any inspection confirmed on AIT.*

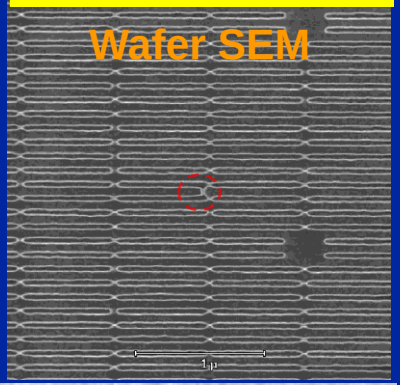
Presented at BACUS 2010

Non-assignable Repeaters detected by AIT

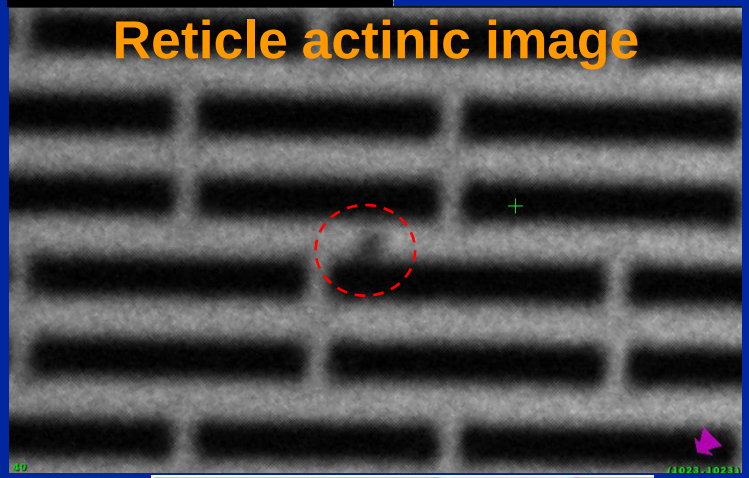
Defect No. 6

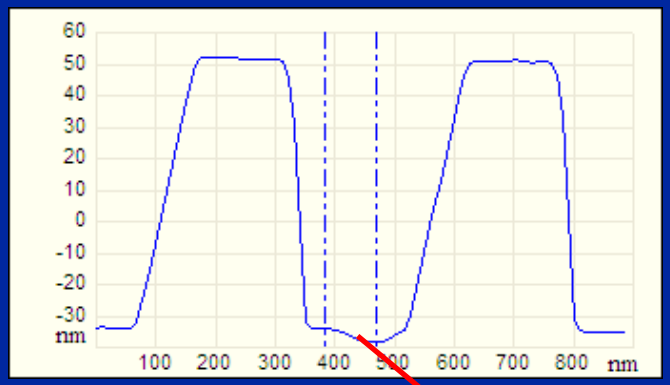


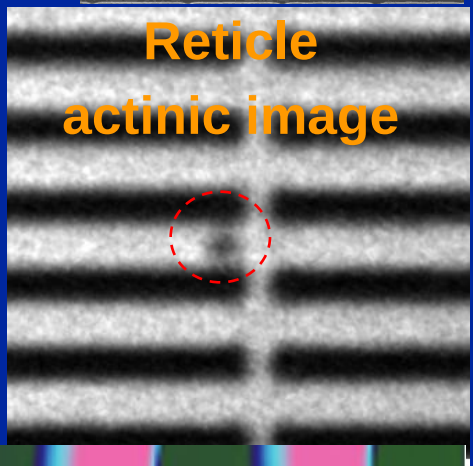
Defect No. 9

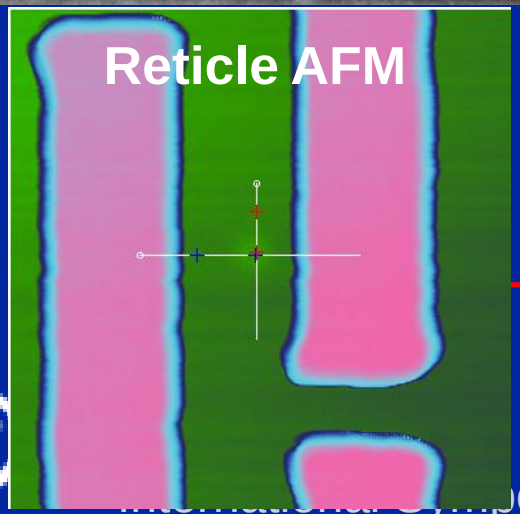


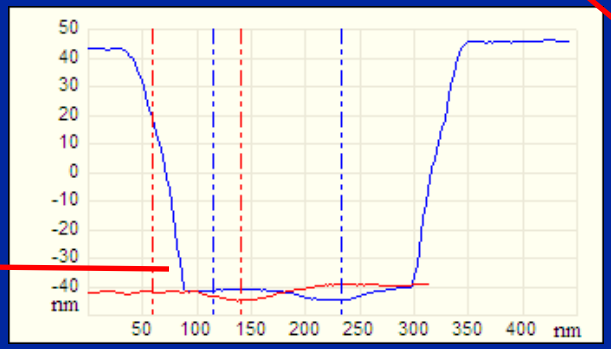
Defects are 3 & 4 nm deep pits (defects 6, 9 respectively).

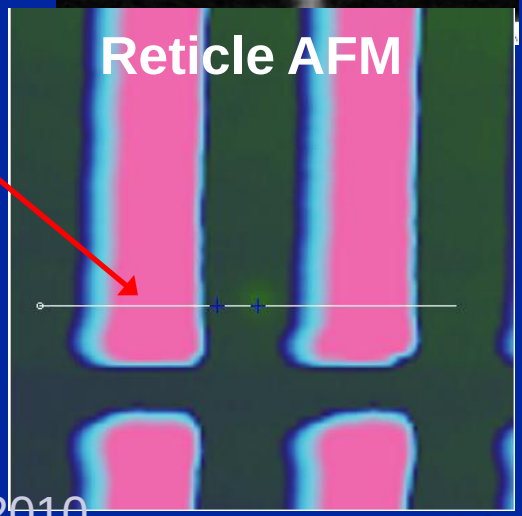




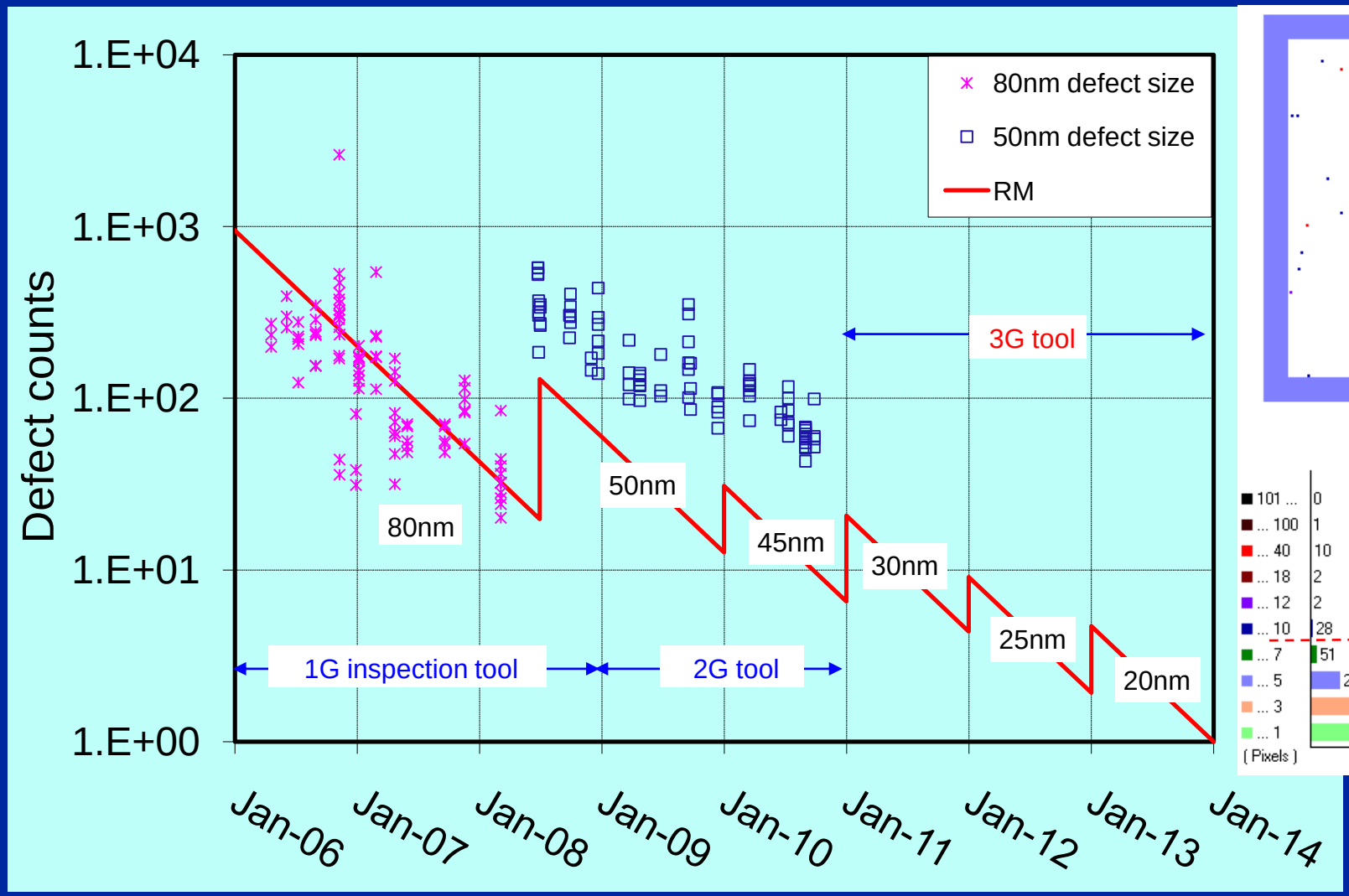


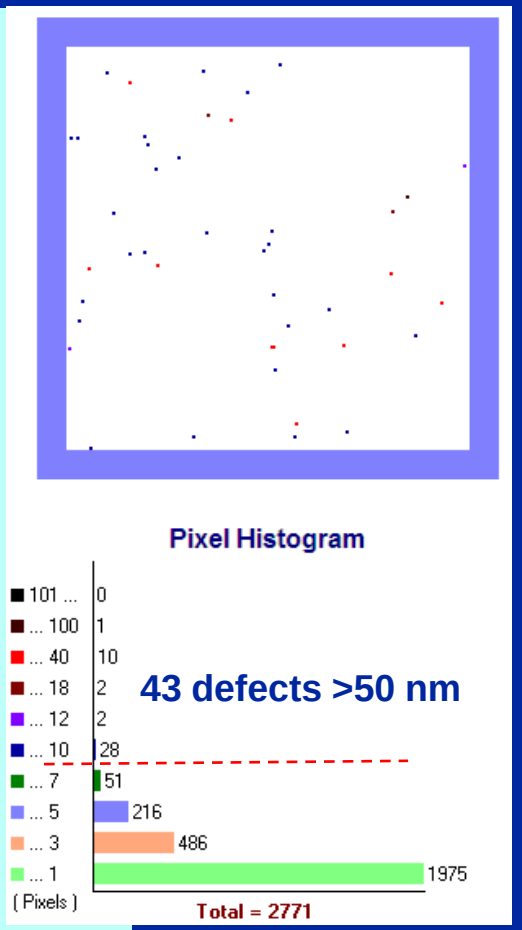






Blank Defect Trend of ML blanks

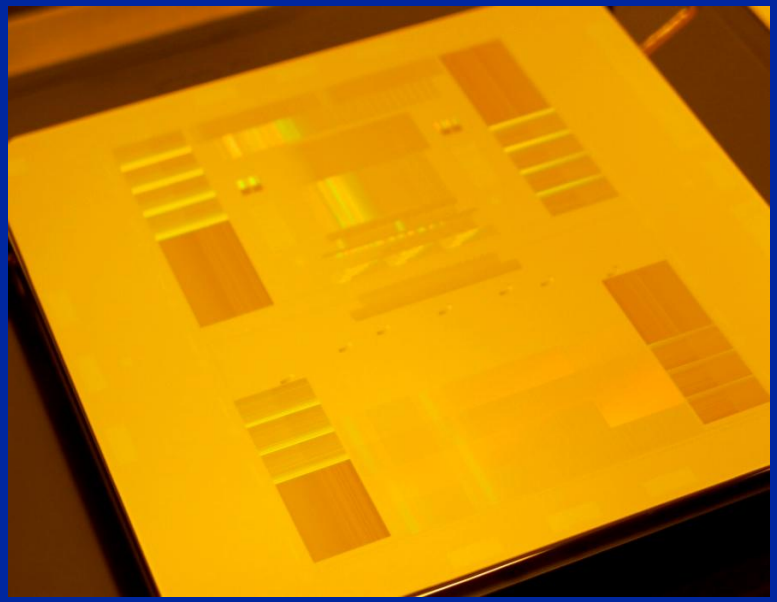


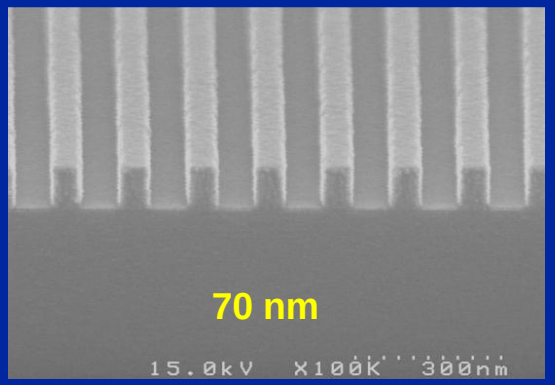


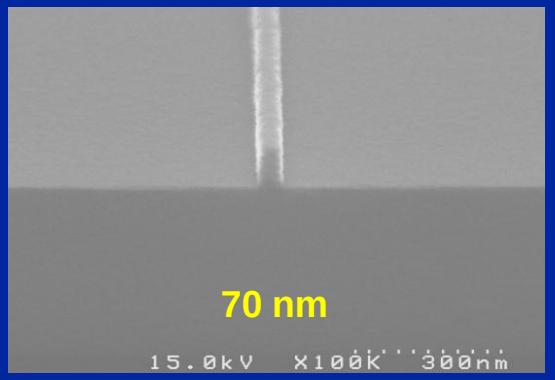
Q3'2010 Blank

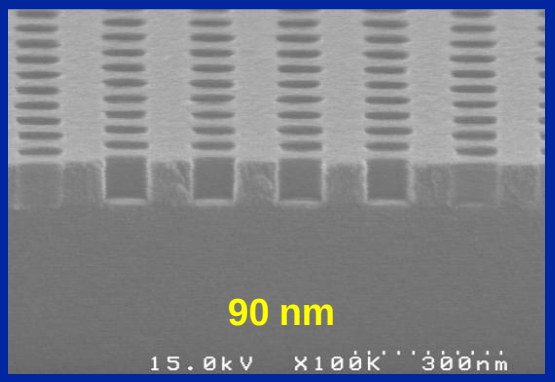
- **"Champion" blank has 43 ML defects @ >50nm (≥pixel 8+)**
- **Challenge is to close the gap to RM**

Mask Patterning Capable to Support 15 nm Node Development

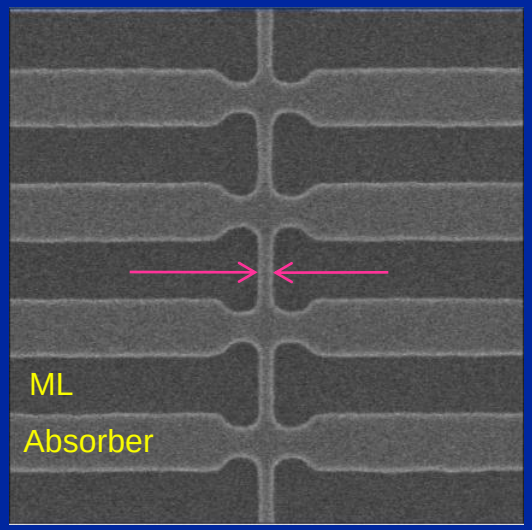




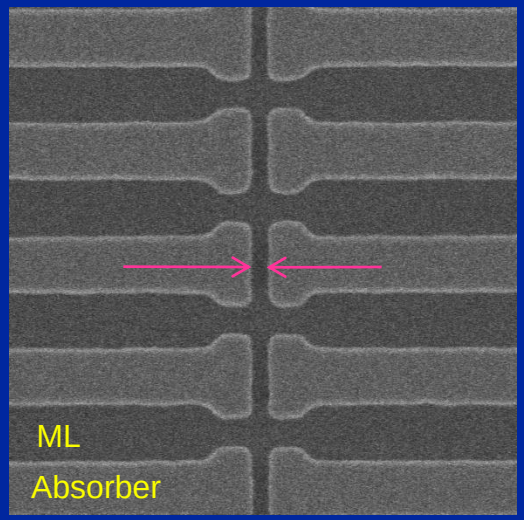




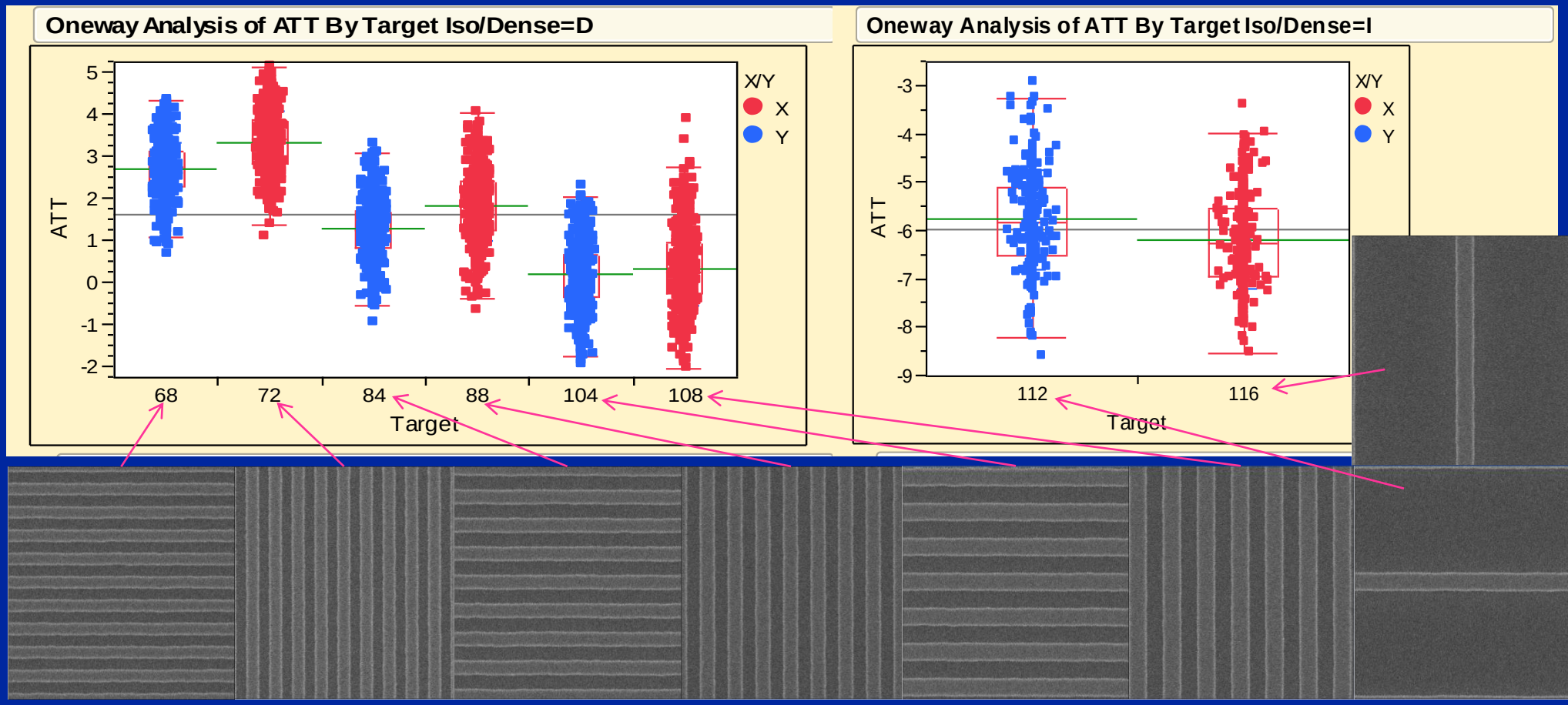
Trench ETE: 40nm



Line ETE: 52nm



Mask CDU Aligned with Expectation

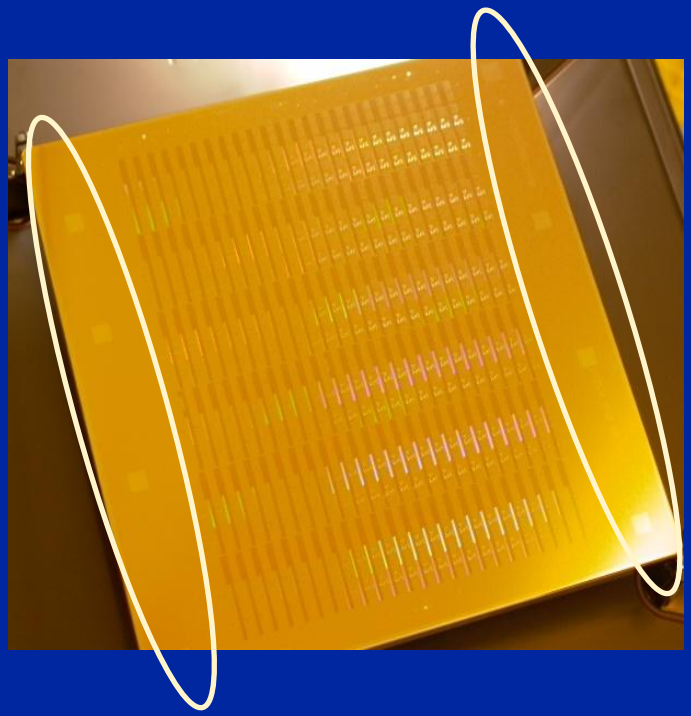


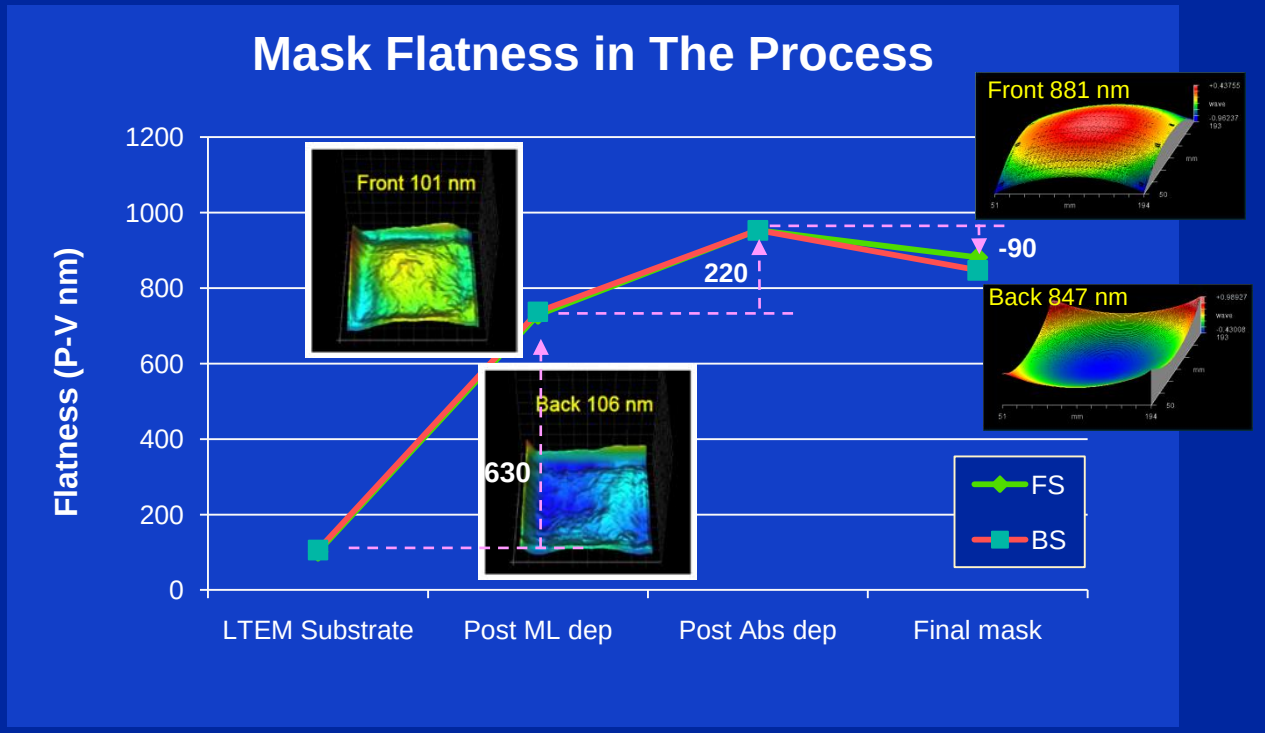
Mask Film Stack

- Substrate: LTEM
- Multilayer: 50 pairs of Mo/Si
- Absorber: 51 nm TaON/TaN
- Backside film: 70 nm CrN

Target CD	Sample size	Mean	6Sigma	CD orientation	Iso/Dense
68	702	2.71	3.88	Y	Dense
72	702	3.35	4.30	X	Dense
84	702	1.28	4.23	Y	Dense
88	702	1.82	4.92	X	Dense
104	702	0.19	4.49	Y	Dense
108	702	0.34	5.31	X	Dense
112	234	-5.77	6.24	Y	Iso
116	234	-6.20	5.87	X	Iso

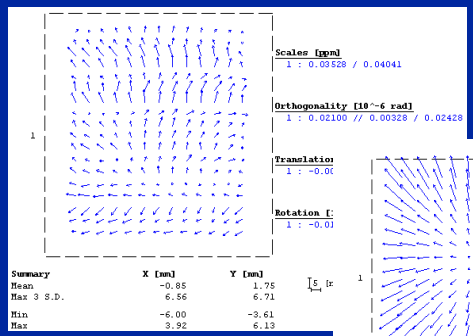
Mask Flatness and EUV Reflectivity Control



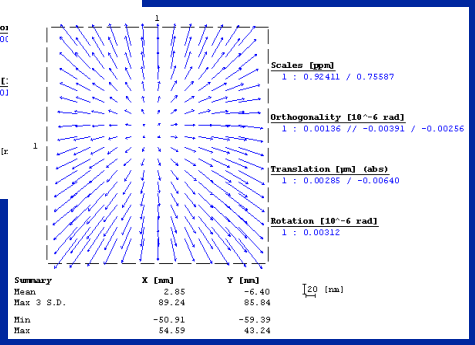


Mask EUV Reflectivity		Blank (7 points)		Mask (7 points)	
		Rp (%)	Centriod λ (nm)	Rp (%)	Centriod λ (nm)
ML	Ave.	63.45	13.523	63.25	13.522
	Max-Min	0.52	0.021	0.133	0.005
Abs				0.54	

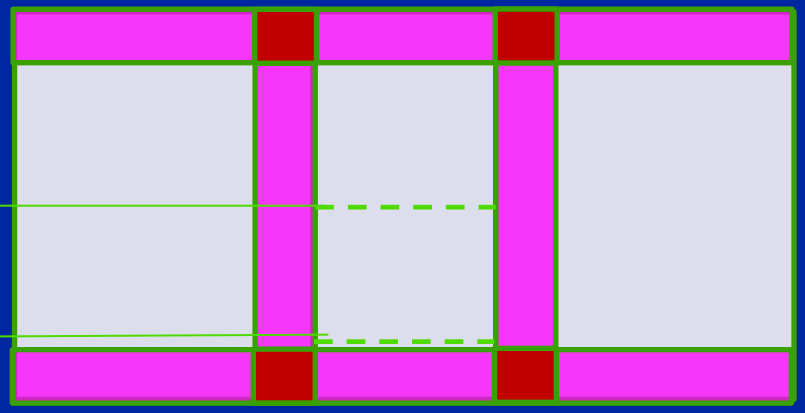
Uncompensated Grid



Compensated Grid

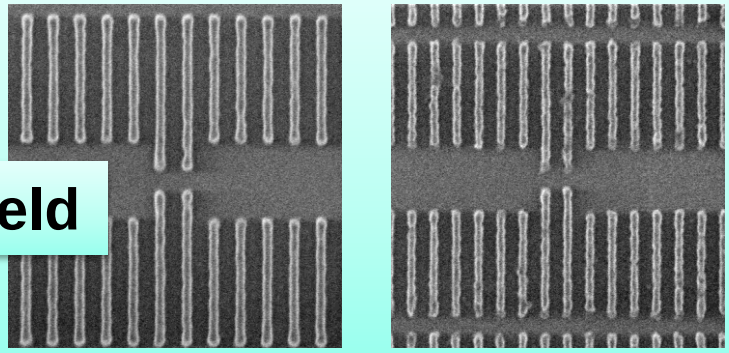


Flare Leakage from REMA and Adjacent Field Have Significant Impact on CD's



2 times exposures (1X undesirable exp.)
4 times exposures (3X undesirable exp.)

Center of the field

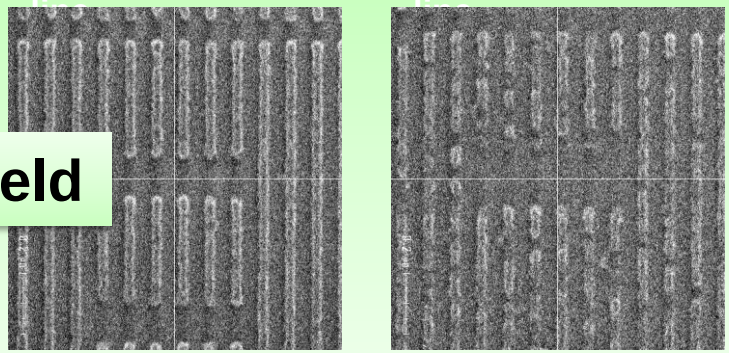


12mm from the edge of scribe

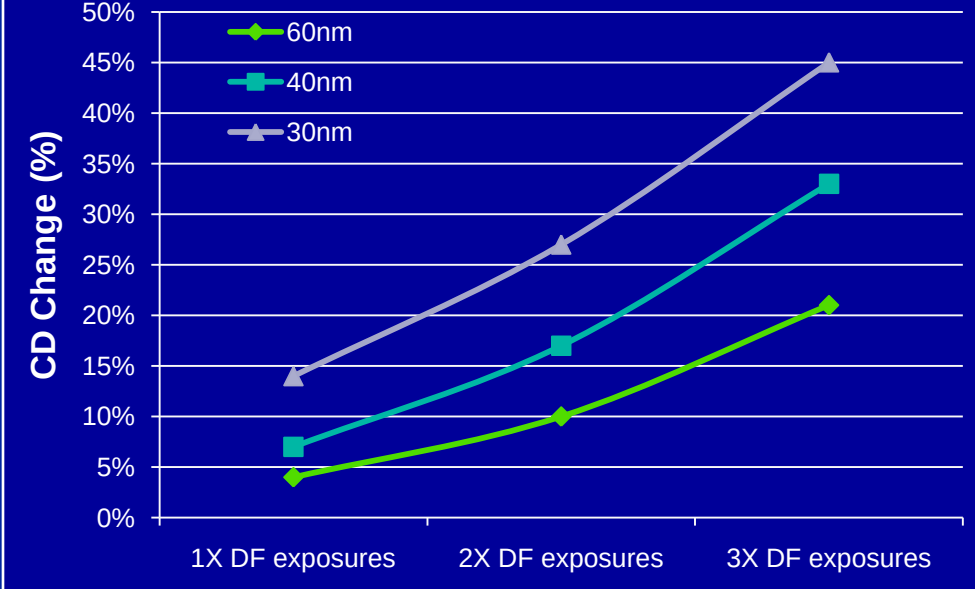
1mm from the edge of scribe

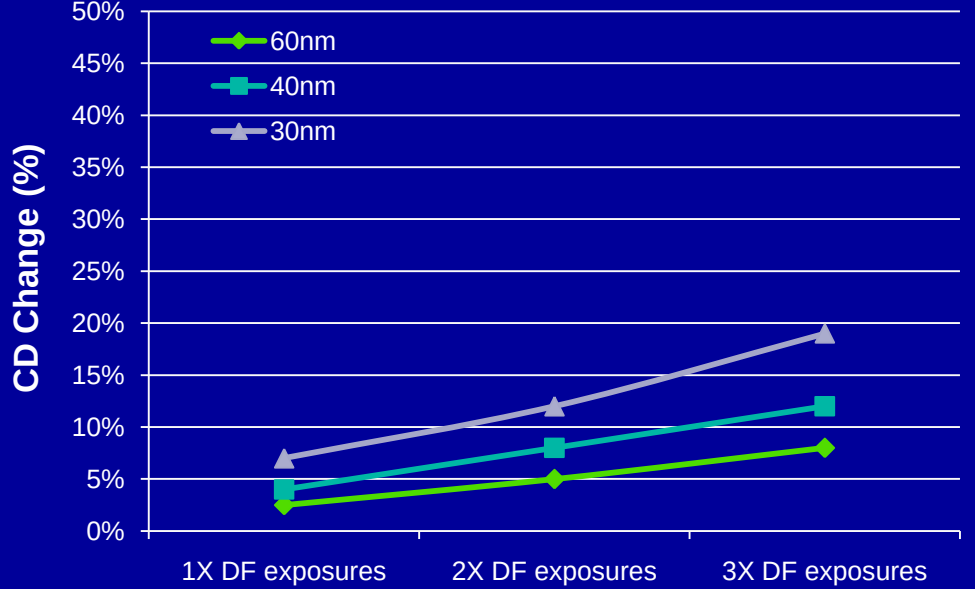
Right at the edge of scribe line

Bottom of the field

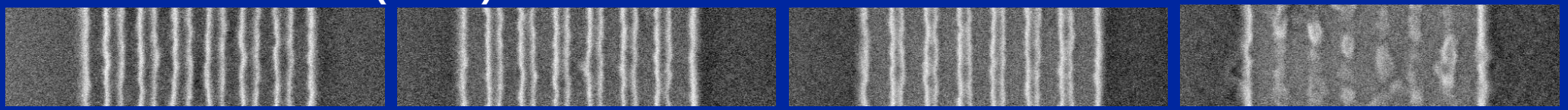


Comparison: CD Change with DF Exp.

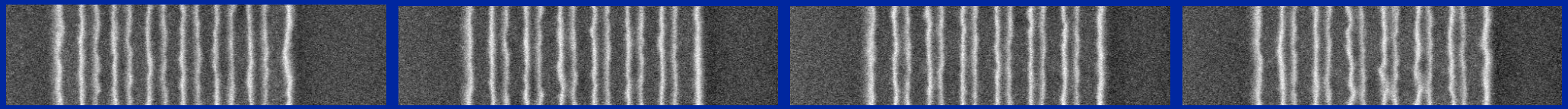




Thin absorber mask (51nm)



Thick absorber mask (87nm)

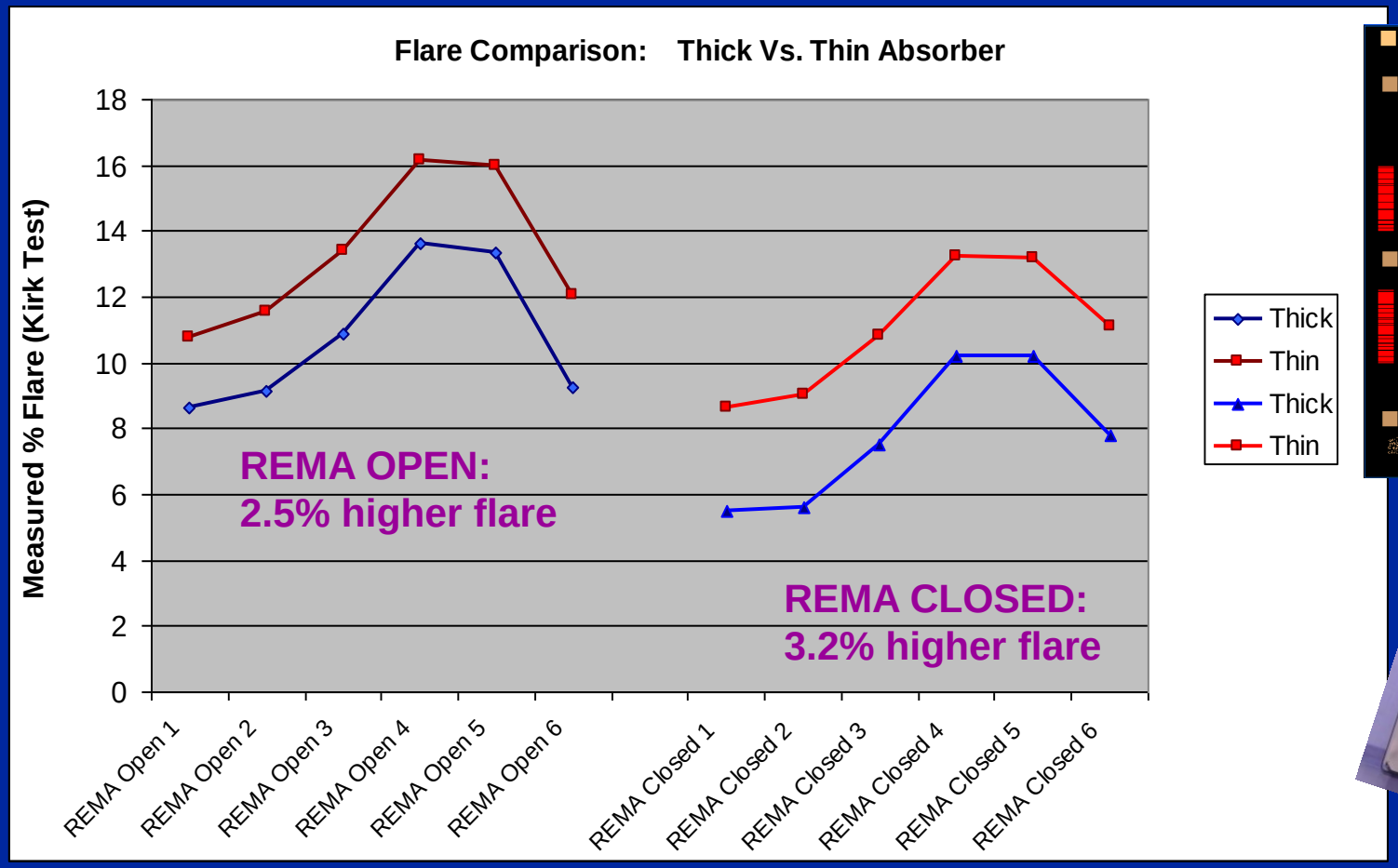


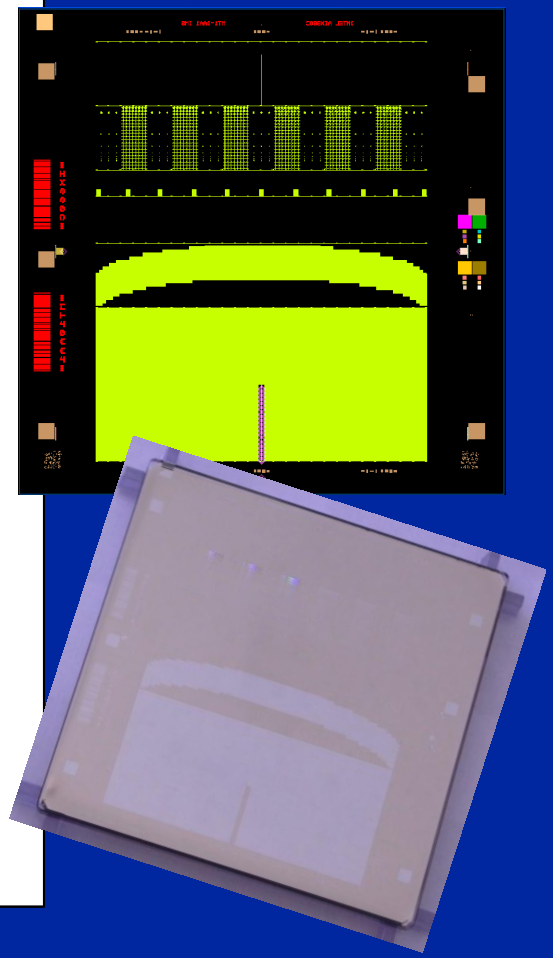
1 exposure | 2 exposures | 3 exposures | 4 exposures

- CD loss quickly with the thin absorber mask

Qualification parameter: MTF (contrast)

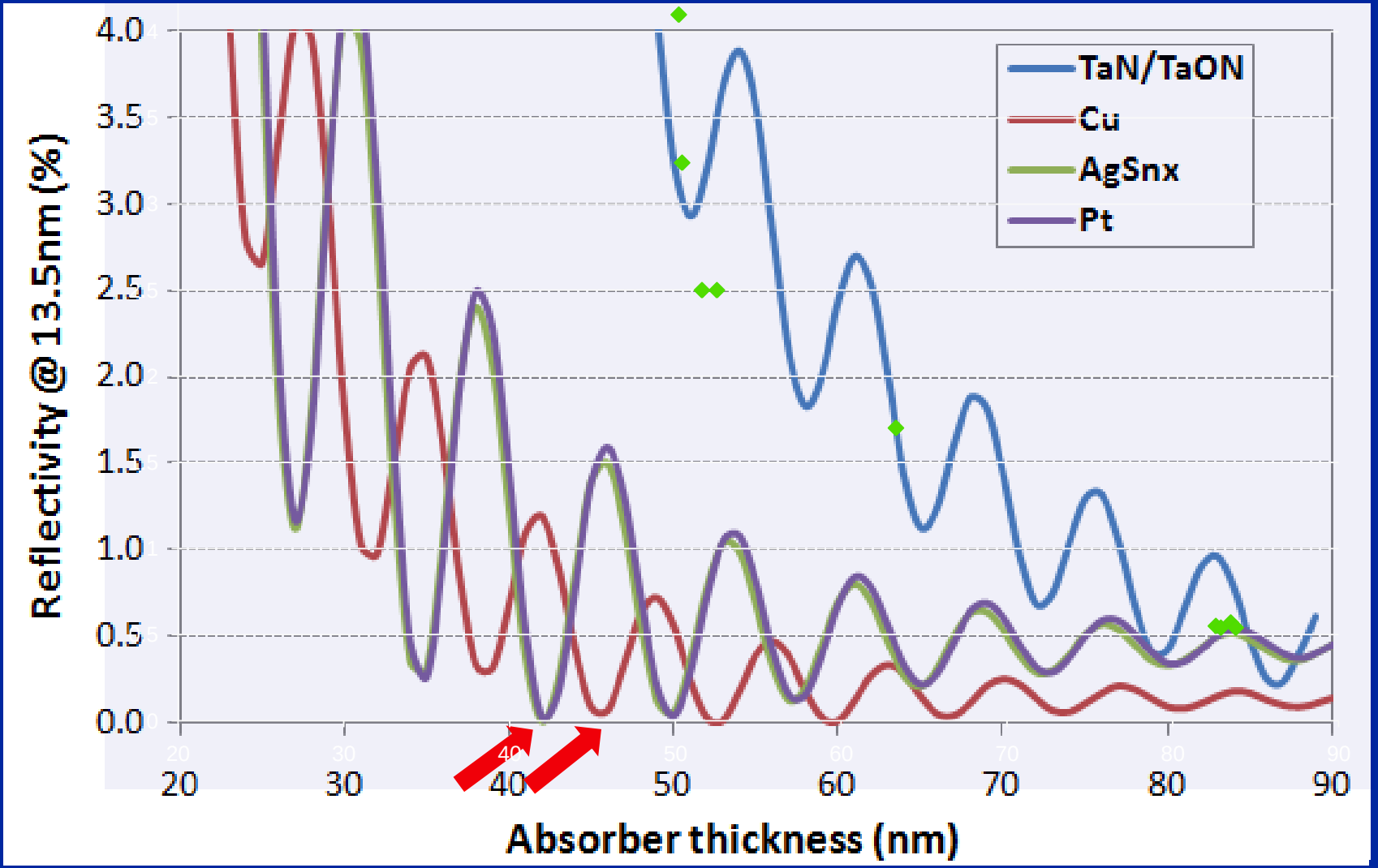
- Thin absorber mask appears to have higher flare due to higher leakage in the absorber.





Higher flare = lower contrast

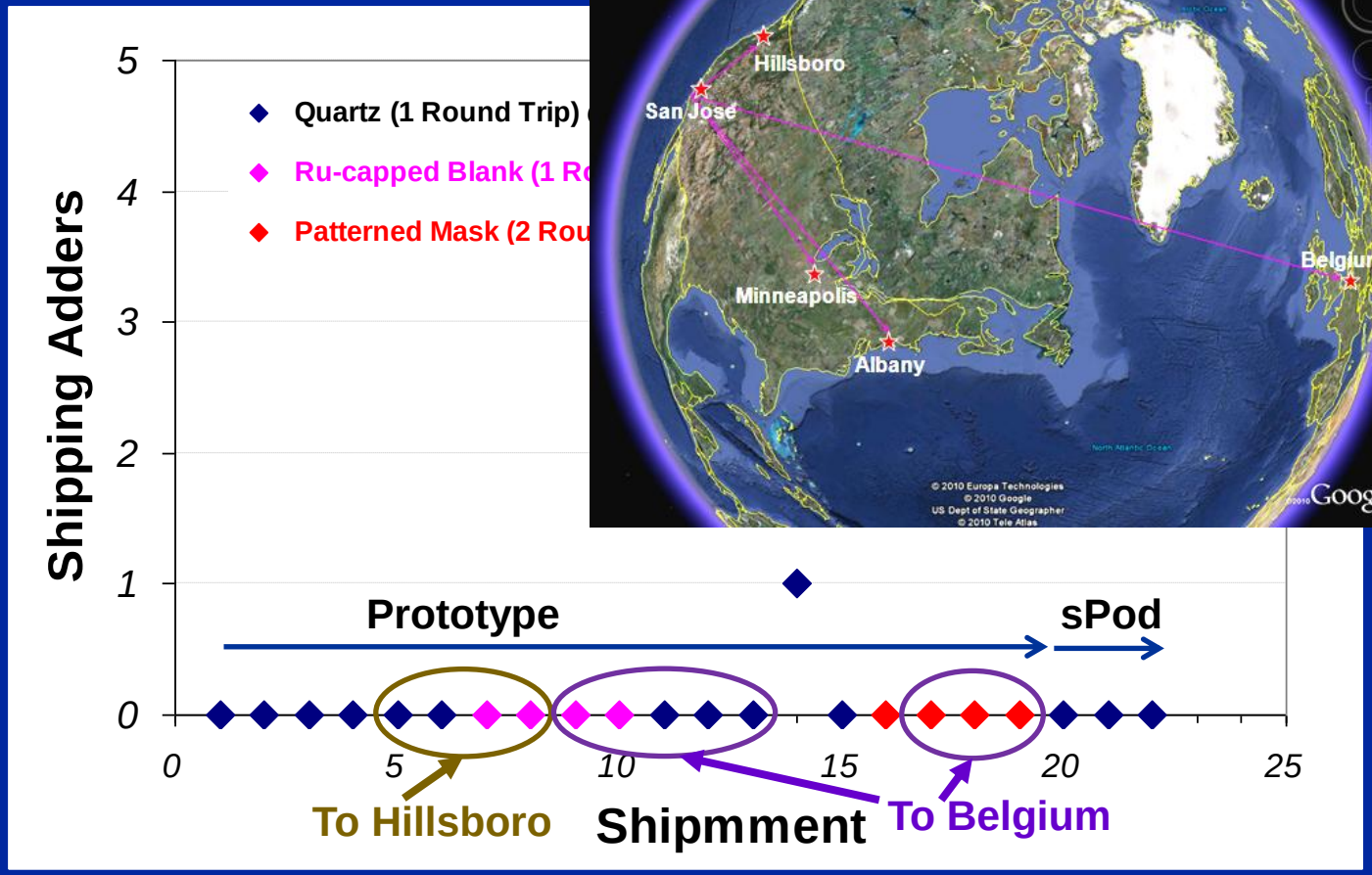
Absorber Thickness Options

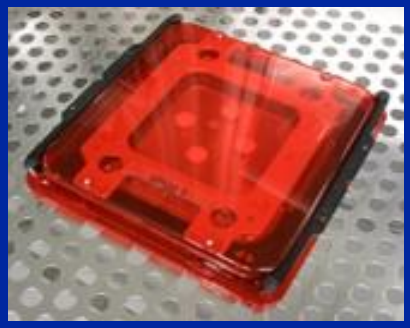


- **Need balance on shadowing effect, EUV leakage, flare, film properties and process integration**

Particle Free Reticle Shipping

- EUV Pod design complies with SEMI std
- Shipping capability/particle control down to ~40nm sensitivity.





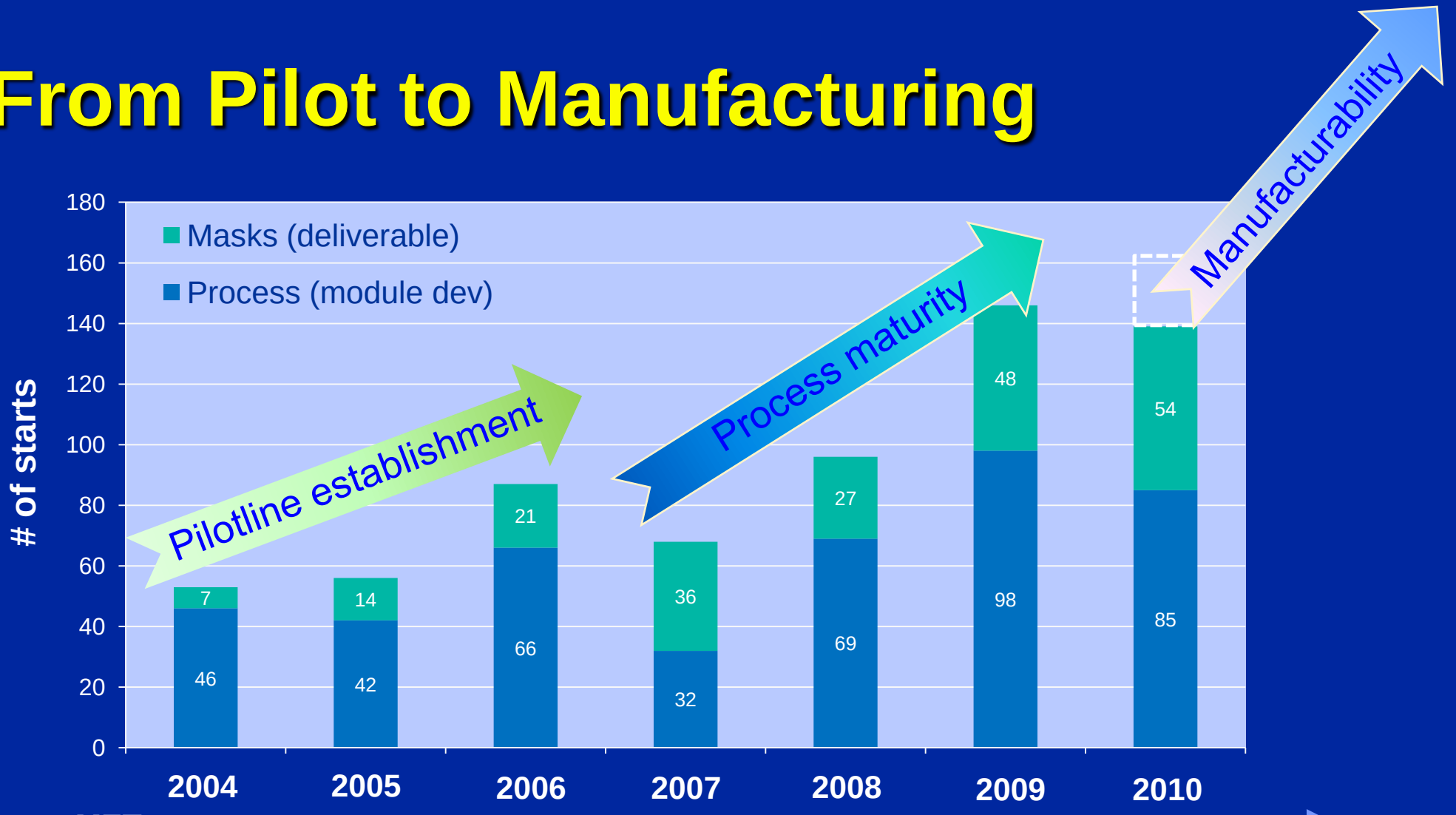
Prototype EUV mask carrier

Product of EUV reticle carrier / sPod

Shipping package with inner and outer box

- EUV Pod works in shipping

From Pilot to Manufacturing



MET
0.3 NA, <3.5% flare, 600 μm field

ADT
0.25 NA, <16% flare

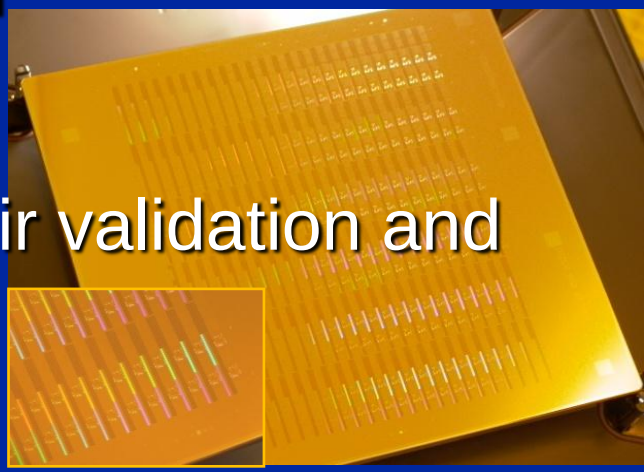
EUV1
0.25 NA, <10% flare

NXE
0.25-0.35 NA, <8% flare

- **Mask development**
- **Tool characterization**
- **Resist evaluation**

Summary

- **Path to defect-free mask**
  - Much progress made in process control, inspection, repair, mitigation and handling
  - Availability of low defect blanks remains challenging
- **Patterning capability**
  - Capable to support 15nm node development
  - Compensation (flare, shadowing, non-flatness) still need to be validated at a device level
- **Infrastructure**
  - Continue focusing on inspection, repair validation and automation



One step closer to HVM

Acknowledgements

Intel IMO: Armando Cobarrubia, Firoz A Ghadiali, Marilyn Kamna, Yan Liu, Kenneth Buckmann and Fabian Martinez

LBNL: Eric Gullikson (reflectometry), Ken Goldberg and Iacopo Mochi (AIT)

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